2024 IITC Workshop and Conference Program

MONDAY, JUNE 3, 2024

Workshop

New dimensions to harness, upside & backside; what to consider and how to control?

Workshop Program:

As the conventional planar scaling of CMOS devices reaches its limits, new directions are being pursued in the vertical dimension to achieve better power, performance, and area (PPA). This shift began with the development of device architectures such as FinFETs, Nanosheets, VTFETs, and StackFETs, which extend or stack up the transistor channels vertical direction. The trend is now expanding to the interconnect/BEOL domain, where the backside of the wafer (BSPDN) and the vertical stacking of semiconductor dies (HBM) are being explored. These vertical integration techniques enable new possibilities for chip design and packaging that can improve PPA. However, they also pose new difficulties in various aspects such as wafer distortion, metrology, defect control, heat management, and reliability. These difficulties must be addressed to ensure the quality and functionality of the devices with novel structures. One of the critical areas that requires more attention is the wafer bonding and thinning process, which affects the lithography process on the wafer backside. Another significant challenge is the heat removal of the bonded wafers that lack the Si substrate. In this workshop, experts from both industry and academia will present and discuss the key technical challenges in detail associated with the 3-dimensional integration of devices, so that the audience can gain more knowledge and insights on this new and important industry trend.

9:00 – 9:15
Welcome & Introduction
Kisik Choi (Chair) – IBM Research

9:15 – 10:00
BSPDN design considerations for advanced logic device
Stanley S.C. Song – Google
Back-side power delivery networks (BSPDNs) is one of key enablers of technology scaling, addressing on-chip power delivery, offering a multitude of benefits for logic devices, including reduced IR drop, increased signal routing freedom, and enhanced design flexibility. This workshop presentation will delve into the details of BSPDN design, including:

- BSPDN Architectures and Implementation Options: Explore various BSPDN architectures, including Power Via, Tap Cell and Back Side Contact approaches with their implementation challenges and trade-offs.

• Impact on Logic Design, Performance, and Thermal Management: Insights into how BSPDNs influence logic design, performance metrics, and thermal considerations for High performance and mobile applications perspective.
• Design Tools, Methodologies, Reliability, and Testing: Understand the specialized design tools and methodologies tailored for BSPDN design, as well as reliability and testing strategies to ensure robust power delivery.

10:00 – 10:45
Delivering Power and Removing Heat; Two challenges that could become the Achilles heel for AI Applicatoins
Madhavan Swaminathan – Penn State University
Heterogeneous Integration (HI) provides the opportunity for dense connectivity between smaller dies from advanced technology nodes to improve yield, provides for connectivity between optimized legacy technology nodes to reduce time to market, and enables the connectivity of dissimilar dies on a single platform to enhance functionality. With emerging applications in artificial intelligence (AI), the power delivery requirements are becoming astronomical while the thermal management solutions are becoming increasingly challenging. These two issues could very well become the Achilles heel for AI applications, unless appropriate solutions are sought and developed using HI.
This presentation will cover some of the emerging challenges in these areas along with solutions being pursued.

10:45 – 11:15 Coffee Break

11:15 – 12:00
Advanced packaging solutions for high performance memory
Kunal Parekh – Micron
The appetite for new applications in computing such as AI, automotive applications, and more efficient computing, are driving the need for memory and logic to rethink the architectures of both processing logic and memory, and resulting in new advanced packaging innovations that enable the future of 2.5D and 3D solutions. In this talk technology enabling interconnect and packaging and solutions will be discussed.

12:00 – 1:00 Lunch

1:00 – 1:45
Wafer bonding: hybrid/fusion bonding
Ilseok Son – TEL
Wafer bonding is one of key modules in 3DI/HI (3D Integration & Heterogeneous Integration) proving for a next generation scaling resolution path through BSPDN (Backside Power Delivery Network) & sequential CFET in logic, 3D Xtacking in NAND flash, multilayer stacking in HBM (High bandwidth memory). In this talk, wafer bonding type, process flow, and challenges in 3DI bonding will be introduced and TEL’s research work on the challenges will be discussed. This discussion covers wide range of topics including incoming wafer condition’s impact on bonding

void & alignment, plasma surface activation modeling & yield impact, bonding alignment impact on e-test with 0.5um pitch hybrid bonding, Cu recess/ oxidation characterization & resolution, Cu anneal expansion modeling, improved bonding energy measurement method, and wafer distortion modeling.

1:45 – 2:30

Backside patterning from lithography perspective: alignment, metrology and overlay control

Michale Kubis – ASML

Lithography resolution has been driving dimensional scaling of semiconductor devices, but nowadays it is more and more complemented with device level 3D architectures (such as Gate-all-around) and system level 3D integration (such as stacked SRAM on Logic). Logic backside power delivery network (BS-PDN) is a disruptive innovation that offers significant performance gain in combination with higher transistor density. Key feature of this technology is the ability to connect to the already fully processed front-end devices from the backside. This connection takes place after fusion bonding and requires, depending on the chosen process flow, a single digit tight post-bonding scanner overlay control.

In this presentation, we will discuss implications of the BS-PDN processing on scanner alignment, overlay metrology, and overlay control for the post-bonding exposures. We will show that a significant improvement is possible to meet the overlay performance requirement by applying high order corrections per exposure of the scanner and we will discuss additional opportunities to improve the performance. We will pay special attention to the wafer edge (R > 135mm) as in this region it will be most challenging to achieve the required post-bonding overlay.

2:30 – 3:00 Coffee Break

3:00 – 3:45

Wafer warpage control by film deposition

Fayaz Shaikh – LAM Research

While high aspect ratio deposition and etching are key enablers for 3D NAND scaling, the combination of increasing the number of layers while controlling wafer bow due to cumulative stress in the film stack has become a major challenge. Such stress-induced wafer distortion has a significant impact on wafer yield due to degraded lithography depth-of-focus, overlay performance, and structural distortion. To improve overall yield, wafer-, die-, and feature-level stresses need to be carefully managed at various steps throughout the entire manufacturing process flow, at times potentially resulting in the preclusion of otherwise performance-enhancing process steps due to their stress characteristics.

Designed to provide a cost-effective solution for controlling wafer bow in 3D NAND manufacturing, VECTOR DT provides a single-step solution for wafer shape management by depositing a tunable counter-stress film on the back of the wafer without contacting the front side, thereby enabling improved lithography results, reduced bow-induced failures, and integration of high performance but highly stressed films. With strong customer adoption since its debut, the VECTOR DT installed base continues to grow as customers are transitioning to more than 200 layers.

This talk will discuss the challenges of wafer shape/warpage in 3DNAND manufacturing and how backside engineering via deposition can solve and manage the wafer shape using VECTOR® DT.

3:45 – 4:30 Roundtable Discussion
Kisik Choi (Chair) – IBM Research, Stanley S.C. Song – Google, Madhavan Swaminathan – Penn State University, Kunal Parekh – Micron, Michale Kubis – ASML, Fayaz Shaikh – LAM Research

4:30 – 4:45 Final Reflections
Kisik Choi (Chair) – IBM Research

TUESDAY, JUNE 4, 2024

Session 1: Conference Kick-off, Awards Program & Keynote
Chair: Zhihong Chen (Purdue University)

8:15 – 8:25
Welcome
Zhihong Chen – Purdue

8:25 – 8:35
Award Program – Best Papers 2023

8:35 – 9:25
Keynote – Technology Innovations to Fuel 1T Transistors
Huiming Bu - IBM
Artificial intelligence (AI) is transforming our world and the demand for computing capability is increasing at an unprecedented pace. Here we will talk about semiconductor technology innovations in logic, memory, and advanced packaging to meet this ever-growing demand in the era of AI. Transistor architecture breakthroughs and integrated circuits interconnects innovations have enabled tens of billions of transistors onto a chip the size of a fingernail. In addition, chiplet and advanced packaging technology will help accelerate technology and design innovation to integrate over 1 trillion transistors onto a single package before the end of 2030. By Increasing the number of transistors on a single package, we can make AI hardware more powerful and more energy efficient.

9:25 – 9:45 Coffee Break

Session 2: Advanced Interconnects I
Chairs: Paul Besser (Entegris) & Tatsuya Usami (Rapidus)

9:45 – 10:15

2.1 Advanced interconnect capacitance and interface engineering beyond 1.4nm Logic Devices (Invited)
Kang Sub Yim – Samsung Electronics

10:15 – 10:45
2.2 Breaking Barriers: Innovations in MOL and BEOL Interconnects for Advanced Semiconductor Technology (Invited)
Gaurav Thareja – Applied Materials

10:45 – 11:05
2.3 Airgap Integration in MP18 Two-Level Semi-damascene Interconnects with Fully Self-aligned Vias
Gilles Delie, Gayle Murdoch, Giulio Marti, Anshul Gupta, Chen Wu, Alicja Lesniewska, Anton Gavrilov, Ivan Ciofi, Souvik Kundu, Stefan Decoster, Seongho Park, Zsolt Tokei – IMEC
Airgap integration in 18 to 26 nm metal pitch (MP) two-metal level semi-damascene interconnects with fully self-aligned vias (FSAV) on 300 mm wafers is reported. The first metal layer (Mx) is patterned using EUV-SADP with subsequent direct metal etch of the Ru film. Airgap is integrated at a targeted height of 4-6 nm below the top metal lines allowing for FSAV compatibility. 80% of kelvin vias landing on Mx at MP18 meet the <50 ohm resistance target specification and 40% of them meet the via-to-line leakage target of <100 pA. The airgap line-to-line capacitance is found to be 40% lower compared to the dielectric gap fill reference.

11:05 – 11:25
2.4 Process Control for the Modification of Ruthenium Resistivity in Scaled Subtractive Interconnects
Jack Rogers, Hirokazu Aizawa, Nicholas Joy, Rinus Lee, Kenichi Imakita, Hojin Kim, Toru Hisamatsu – TEL Technology Center, America, LLC
For advanced interconnect nodes, finding a new low-resistivity, barrier-independent material to replace copper becomes critical as pitch scaling reaches less than 20nm due to the poor scaling of barrier/liner films necessary for copper metallization leading to increased resistivity. Materials like ruthenium are promising replacement interconnects since they can be barrier-less and have good electrical properties at narrow wire dimensions. However, ruthenium film properties can vary depending on the underlayer and film deposition conditions. Optimization of the ruthenium deposition process is therefore necessary to provide a sufficient advantage over copper. Film grain size and orientation both impact resistivity, and the modification of these parameters is discussed and presented in this report.

11:25– 11:45
2.5 Interface engineering for performance and reliability boosting of logic devices
Jong Min Baek, Suhyun Bark, Yeonggil Kim, Minchul Ahn, Geun Tae Yun, Deokyoung Jung, Hoon Seok Seo, Sungsoo Kim, Kyuhee Han, Youngwoo Cho, EunJi Jung, Taehong Ha, Kang Sub Yim, Sunjung Kim – Samsung Electronics
As the width of interconnects decreases, it is getting more crucial to figure out and handle interfacial phenomena, which is called as interface engineering, to ensure device performance

and reliability. In this study, we investigated various interactions among metal to metal and metal to dielectric interfaces in interconnect structure with regard to electrical characteristics related to resistance, capacitance, and reliability. As a result, it enabled to improve in resistance by ~30% and capacitance by ~5% via recently developed and optimized process conditions in sub-2nm logic devices.

11:45 – 1:20 Lunch

Session 3: Reliability & Failure Analysis
Chairs: Kuan-Neng Chen (Tokyo Institute of Technology) & Munehiro Tada (Nanobridge Semiconductor)

1:20– 1:40
3.1 Intrinsic Reliability of High Capacitance Density Topographic MIM
Christopher Perini, James Palmer, Shahriar Imam, Neena Gilda, Che-yun Lin, Rahim Kasim, James Waldemer, Chris Pelto – Intel Corporation
Addressing the ever-increasing demand for efficient power integrity requirements necessitated the advent of on-die decoupling capacitors. These capacitors provide high dynamic current throughout switching workloads and reduce power supply droop during microprocessor operation. In this paper, we demonstrate a high reliability Metal-Insulator-Metal (MIM) decoupling capacitor on patterned topography with best-in-class capacitance density, implementable in a standard BEOL stack. Conduction behavior through the HiK dielectric is investigated along with complete characterization of Time Dependent Dielectric Breakdown (TDDB). The MIM capacitor reliability exhibits an intrinsic lifetime of >10 years at 1.32 V operation at 125°C. In addition, this process demonstrates excellent low extrinsic defect density and meets standard JEDEC environmental Reliability requirements. The combination of high capacitance and robust reliability of the integrated topographic MIM process significantly enhances the efficiency of on-chip power delivery and protects against power supply noise.

1:40– 2:00
3.2 Investigation of Cu barrier properties of 1-nm-thick PVD-Co(W) films as a single liner/barrier in next-generation ULSI-Cu interconnect
Yubin Deng, Takeshi Momose, Yukihiro Shimogaki – University of Tokyo
In this study, a quantitative evaluation of Cu barrier properties with different thicknesses and compositions of ultrathin physical vapor deposited (PVD) Co(W) films was conducted through a comprehensive analysis using the modified time-lag method. Compared to the 20-nm-thick PVD-Co(W) films, which crystallized after annealing, the PVD-Co(W) films with 1~3-nm-thickness remained amorphous and exhibited enhanced barrier properties. The amorphous structure of the thinner films improved the barrier properties by eliminating the grain boundaries as the primary diffusion path for Cu atoms. More importantly, a 1-nm-thick PVD-Co(W) film with a W composition of 35 at. % exhibited exceptional Cu diffusion barrier properties, surpassing other compositions. This superior performance can be attributed to the high thermal stability that preserves the amorphous structure and overall integrity of the film, resulting from the optimal atom packing. This film also displayed the lowest Cu diffusivity (D)

and highest activation energy (Ea = 2.5 eV) among all the investigated barrier candidates. In addition, ultrathin PVD-Co(W) films can function effectively as both a barrier against Cu diffusion and an oxygen diffusion block, underscoring their application superiority to Cu interconnects in next-generation ultra-large-scale integration (ULSI) devices.

2:00– 2:20

3.3 Assessing Impact of Non-Uniform Localized Heating on Reliability

Yoon Jo Kim, Edwin B. Ramayya, Lei Jiang, Jason Jopling, Rahim, Kasim – Intel Corporation

Moore's Law-driven technology improvements have led to a significant increase in power density across a multitude of market segments, from mobile to HEDT (high-end desktop) and servers. This, in turn, has led to an increase in both spatial and temporal thermal non-uniformity across the chip. In this paper, thermally-induced reliability risks due to localized heating (thermomigration and thermal fatigue) were experimentally investigated. Novel test structures as well as experiments were devised to assess these risks. Thermomigration risks were demonstrated to be low at power densities up to 370°C/μm. The assessment of local thermal fatigue risks for contact- M4 layers indicated that they exhibited no failures through up to 10 billion thermal cycles, within peak temperature ranges of 220°C to 280°C.

2:30– 2:40

3.4 Highly Reliable Ruthenium-Cobalt Binary Liner for Advanced Node Cu interconnect

Gyuho Myeong, Junki Jang, Kihyun Kim, Jaeho Lee, Eunyoung Park, Hoyun Jeon, Kyounghee Nam, Eunji Jang, Chin Kim, Doowhan Park, Rak-Hwan Kim, Jeonghoon Ahn and Jongho Lee – Samsung Electronics

In this paper, alternative Ruthenium-Cobalt Binary Liner (RCBL) instead of conventional Co liner with atomic layer deposition (ALD) TaN barrier metal was studied. ab initio simulation shows Co liner has various phases with different Cu wettability and its phase ratio with high wettability increases with Ru substrate rather than Ta substrate. Additionally, adhesion between barrier metal and liner increases in RCBL as lattice mismatch decreases. As a result reduction in 87% of Cu void and 14% of line resistance were achieved in relatively thin RCBL with high Cu wettability compared to conventional Co liner process. Manufacturability and reliability of RCBL process were also confirmed with logic chip yield and time dependent dielectric breakdown (TDDB) measurement of foundry product for advanced node.

2:40– 3:00

3.5 Impact of ESD Events on TSV Liner Reliability

Emmanuel Chery, Michele Stucchi, Stefan, Van Huylenbroeck, Eric Beyne – IMEC

In this work, 0.7μm via-last TSV arrays were pre-stressed with a series of ten 60 V ESD pulses. Their liner reliability performances were subsequently investigated though voltage ramp stresses with various ramp rates to assess the impact of the ESD pre-stress on the dielectric properties. The breakdown voltage and leakage current of pre-stressed structures is unaffected by the ESD events.

3:00 – 3:20 Coffee Break

Session 4: Metrology & Patterning
Chairs: Mark Zaleski (Micron) & Benjamin Lilienthal-Uhlig (Fraunhofer Inst.)

3:20– 3:50

4.1 Resolving nanoscale composition fluctuations and defects in advanced interconnects: a crucial step to comprehend thin film resistivity (Invited)

Claudia Fleischmann – IMEC

3:50– 4:10

4.2 Advanced Black Diamond® for <2nm BEOL Low k Integration

Bo Xie, Rui, Lu, Orlando Trejo, Akansha Singh, Michael Haverty, Lauren Bagby, Kent Zhao, Lakmal Kalutarage, Monika Jamieson, Chi-I Lang, Chandru Ramalingam, Li-Qun Xia – Applied Materials

The scaling of <2nm technology node is extremely challenging. It demands a robust low k for BEOL integration due to the reduced cross-sectional area of metal wires which increases the resistance-capacitance (RC) of BEOL interconnects. Realizing this aggressive pitch is challenged by variability and mechanical stability issues and an increasing process flow complexity. The electrical and mechanical property requirements of low k dielectrics are crucial though to enable a variety of new process innovations, scaling boosts, and new conductors for interconnect scaling.

4:10– 4:30

4.3 Low-Resistivity Subtractive-Etched W Lines and Highly Reliable High Aspect Ratio Fully Self-Aligned Vias for 3D Flash Memory

Mitsuhiko Noda, Genki Sawada, Seiya Hirano, Sota Araki, Atsushi Rikukawa, Yusuke Goki, Katsumi Yamamoto, Toshiyuki Sasaki, Daichi Nishikawa, Toshiyuki Morita, Masayoshi Tagami, Norio Ohtani, Masaru Kito – Kioxia Corporation

A novel process integration of low-resistivity subtractive-etched tungsten (W) interconnect and high aspect ratio fully self-aligned vias (HAR-FSAV) have been developed for 3D flash memory. The low-resistivity W line is achieved through surface treatment after the subtractive etching process. The HAR-FSAV is constructed by introducing a stacked interlayer dielectric structure and optimizing upper via etching condition. These technologies are promising for shrinking the interconnects of 3D flash memory in the future.

4:30– 4:50

4.4 A novel single damascene process for via metal corrosion-free interconnects in advanced nodes

Koichi Motoyama, Dominik Metzler, Jennifer Church, Hosadurga Shobha, Haojun Zhang, Huai Huang, Kisik Choi – IBM Research

Via metal corrosion during via CMP is one of the major process challenges for S/D (single damascene) interconnects. Thus, the detailed mechanism of via metal corrosion during via CMP have been investigated and a novel via process has been proposed to demonstrate via metal corrosion-free S/D interconnects. The via metal corrosion-free S/D interconnect could achieve improved viachain yield and enhanced EM (electromigration) performance compared to D/D (dual damascene) interconnect due to an ideal via profile and better Cu fill capability.

WEDNESDAY, JUNE 5, 2024

Session 5: Keynote
Chair: Zhihong Chen (Purdue University)

8:15 – 9:05
Keynote – Materials Challenges for the Semiconductor Industry
Dr. James O'Neill – Entegris

Session 6: Advanced Interconnects II
Chairs: Todd Ryan (Intel) & Kang Sub Yim (Samsung)

9:05 – 9:35
6.1 Advanced Logic Interconnect: Challenges and Potential Solutions (Invited)
Harsono Simka – Samsung Electronics

9:35 – 9:55
6.2 A Rapid Process for Vapor-deposited MOF as low-k dielectrics seamless gap fill for M1 and M2 Interconnects
Dipayan Pal; Naeun Yang, Harsono Simka, Andrew Kummel – UC San Diego, Samsung Electronics
A rapid novel process of vapor phase ZIF-8 MOF deposition is reported with commercially viable process time (15 min only) at 160C CVD temperature. This is the fastest reported vapor process to form a MOF film, and it was enabled by the high processing temperature and a low background H_2O environment. Both high aspect ratio gap fill and multiple aspect ratio gap fill were demonstrated; this is the first report of multiple aspect ratio gap fill with no residual ZnO remaining. Parallel plate capacitors were fabricated, and k value was estimated to be ~2.6, and the devices were stable over months. Applications can be found in BEOL, FEOL device fabrication, packaging, and three-dimensional heterogeneous integration (3DHI).

9:55 – 10:15
6.3 Exploration of Barrier Materials for Cu_2Mg/SiO_2 and resistivity scaling of twinned Cu_2Mg ***(Student Paper)***
Toshihiro Kuge, Masaya Iwabuchi, Mansour Moinpour, Ravi Kanjolia, Masataka Yahagi, Junichi Koike – Tohoku University, EMD Electronics
Cu_2Mg shows a slow resistivity increase with decreasing film thickness below 10 nm. However, Mg has a strong tendency to react with dielectric oxide and degrade the property of the interconnect structure. This work explored a barrier material to prevent the reaction and to find a reason to maintain a low resistivity below the film thickness of less than 10 nm. The results showed a good barrier property of 1nm Mo, 2nm Ru, and 2 nm Y_2O_3, which agreed well with thermodynamic calculation. The good resistivity scalability was attributed to easy twinning tendency in a C15 cubic Laves phase.

10:15 – 10:35 Coffee Break

Session 7: Materials & Unit Process I
Chairs: Soo-Hyun Kim (Yeungnam University) & Benjamin Lilienthal-Uhlig (Fraunhofer)

10:35 – 11:05
7.1 Atomic Layer Deposition of Molybdenum for barrierless metallization of Vias and Lines (Invited)
Jans Willem Maes – ASM

11:05 – 11:35
7.2 Interconnects Patterning: Novel Innovations and Challenges (Invited)
Florian Gstrein – Intel

11:35 – 11:55
7.3 Two Metal Level Semi-Damascene Interconnects for Superconducting Digital Logic
Sara Iraci, Ankit Pokhrel, Daniel Perez Lozano, Jean-Philippe Soulie, Sujan Kumar Sarkar, Rajendra Kumar Saroj, Yann Canvel, Vincent Renaud, amey walke, Bart Kenens, Blake Hodges, Seifallah Ibrahim, Trent Josephsen, Benjamin Huet, Gayle Murdoch, Min-Soo Kim, Sabine O'Neal, Quentin Herr, Anna Herr, Zsolt Tőkei – IMEC
In this paper we present a superconducting two-metal level (2ML) BEOL unit process based on NbxTi(1-x)N (NbTiN) that was developed in imec's 300 mm pilot line using a semi-damascene flow and 193i lithography. The unit process features direct-metal-etch wires with minimum critical dimension (CD) of 50 nm and shallow planarized vias with minimum CD of 80 nm deposited at 420 °C, compatible with CMOS BEOL dielectrics. Normalized line resistance of 50 nm NbTiN wires show that 95% of the devices meet the expected resistance 800-1200 Ω/µm consistent with blanket films resistivity. Low temperature measurements show that NbTiN wires and vias have a critical temperature of 12-13.5 K and a critical current density of 80-113mA/µm2.

11:55 – 12:15
7.4 Barrier-Less W Metallization Processes for Low-Resistance Contacts at Sub-3 nm Logic Devices
Seongdong Lim, Seongheum Choi, Jeongik Kim, Byungchul Kang, Daeun Kim, Yeji Song, Donghyun Kim, Sanghoon Uhm, Chunghwan Shin, Taehong Ha – Samsung Electronics
The low-resistance of middle of line (MOL) contacts has been highlighted as critical for high-performance logic devices. Tungsten (W) has been widely used in MOL, but the relevantly required barrier materials (e.g. TiN) prevented achieving low resistance contacts as the dimension shrinks down. The replacement of high resistance barrier by an enhanced PVD W technology with an excellent step coverage allowed barrier-less W process, but a limited gap-fill performance of PVD W alone is still challenging for ultra-high aspect ratio contacts at sub-3 nm logic devices. In this study, a novel fabrication route of low-resistance barrier-less W contacts has been freshly demonstrated by reinforcing the combination of PVD W and CVD W with an

adoption of nucleation process. The result of ASTAR TEM analysis exhibits a single crystallographic orientation in each contact, which is desirable for the low resistivity and reliability. Furthermore, the nucleation-assisted barrier-less W shows dramatically reduced contact resistance compared to the conventional W metallization with barrier, which resulted in significant gain of AC performance in logic devices. The suggested barrier-less W metallization process is strongly believed to be more efficiently applicable to high-performance sub-3 nm logic devices.

12:15 – 1:30 Lunch

Session 8: Contacts to CMOS Devices & Novel/Emerging Technologies
Chair: Philippe Rodriguez (CEA-Leti) & Mansour Moinpour (EMD Electronics)

1:30 – 2:00

8.1 Programmable Optics Based on Copper Interconnects for Lidar, Communications, Optical Computing, and Beyond (Invited)

Gleb Akselrod – Lumotive

Light Control Metasurface (LCM^{TM}) devices using Cu pillars as resonators have been successfully developed and commercialized for the first time for solid-state optical beam steering in 3D sensing applications. In contrast to conventional Cu interconnect applications in logic or memory devices where Cu is used because of its low resistivity and great electromigration performance, Cu is chosen as the pillar material in the LCM^{TM} device thanks to its excellent optical properties. The Cu pillars are fabricated using conventional Cu damascene processes followed by patented integration scheme to remove the dielectric material between Cu lines. The solid-state beam steering is achieved by applying different voltage patterns to the Cu pillars without any mechanical moving parts, leading to superior reliability performance. The LCM^{TM} device can generate a wide field of view (FOV) beam steering larger than 160°. The beam can be steered from one direction to another direction within microseconds. The unique capability of the LCM device combined with low costs of the fabrication process make it a leading candidate for 3D sensing lidar applications. Furthermore, the LCM^{TM} device has the potential in a wide range of new applications such as optical communications, computing, and beyond.

2:00 – 2:30

8.2 BEOL based memristive devices and circuits for energy efficient artificial neural networks (Invited)

Sven Zimmerman – Fraunhofer ENAS

2:30 – 2:50

8.3 Front-side Integration of Middle-of-line Stacked Contacts for Monolithic CFET

Victor Vega Gonzalez, Karen Stiers, Cassie Sheng, Steven Demuynck, Camila Toledo de Carvalho Cavalcante, Lucas Petersen Barbosa Lima, Thomas Chiarella, Juergen Boemmels, Tanushree Sarkar, Nathali Franchina Vergel, Dunja Radisic, Roger Loo, erik rosseel, Clement Porret, Geert Mannaert, Subhobroto Choudhury, Vincent Brissonneau, Emmanuel Dupuy, Anthony Peter, Nicolas Jourdan, Jean-Philippe Soulie, Takahiro Hakamata, Ainhoa Romo Negreira, Robert Clark,

Kevin vandersmissen, Farid Sebaai, Pallavi Puttarame Gowda, Ju Geng Lai, Sunil Kumar Sanjeevi, Andrea Mingardi, Chan BT, Alfonso Sepulveda Marquez, Robert Langer, Il Gyo Koo, Efrain Altamirano Sanchez, katia devriendt, Paulina Rincon Delgadillo, Frederic Lazzarino, jerome mitard, Jef Geypen, Dmitry Batuk, Yi Fan Chen, Frederik Verbeek, Frank Holsteyns, Sujith Subramanian, Zsolt Tokei, Naoto Horiguchi, Serge Biesemans – IMEC
A 200nm-pitched, superconducting niobium (Nb) interconnects with TiN protecting layer are fabricated on a 300-mm wafer for cryo-CMOS used in Quantum State Controller (QSC) application. The developed Nb interconnects show superior superconductivity with a Tc of 7.8 K and a record-high Jc of 64MA/cm2 at 4.2 K, which is high enough to local interconnects used in a cryo-CMOS circuit. For the first time, the SPICE simulation, using a 65nm-node cryogenic (4K) PDK with a technology file including Nb superconducting interconnects, estimates 40% improvement in signal delay in a typical use case. This result indicates that a cryogenic CMOS operation power can be reduced by the superconducting interconnects, as the operating voltage can be lowered while maintaining the same operation speed as that with the Cu interconnects.

2:50 – 3:10

8.4 200nm-pitched, Superconducting Nb Interconnects for Cryo-CMOS Application

Noriyuki Iguchi, Hideaki Numata, Masamitsu Tanaka, Koichiro Okamoto, Takahisa Tanaka, Ken Uchida, Hiroki Ishikuro, Toshitsugu Sakamoto, Munehiro Tada – NEC Corporation, Nagoya University, NanoBridge Semiconductor, Inc., Keio University, The University of Tokyo
A 200nm-pitched, superconducting niobium (Nb) interconnects with TiN protecting layer are fabricated on a 300-mm wafer for cryo-CMOS used in Quantum State Controller (QSC) application. The developed Nb interconnects show superior superconductivity with a Tc of 7.8 K and a record-high Jc of 64MA/cm2 at 4.2 K, which is high enough to local interconnects used in a cryo-CMOS circuit. For the first time, the SPICE simulation, using a 65nm-node cryogenic (4K) PDK with a technology file including Nb superconducting interconnects, estimates 40% improvement in signal delay in a typical use case. This result indicates that a cryogenic CMOS operation power can be reduced by the superconducting interconnects, as the operating voltage can be lowered while maintaining the same operation speed as that with the Cu interconnects.

3:10 – 3:30

8.5 Fabrication of Superconducting Nb Airbridges in a 300 mm Pilot Line for Quantum Technologies

Danny Wan, Massimo Mongillo, Yann Canvel, Daniel Perez Lozano, Bert Tobback, Tsvetan Ivanov, Antoine Pacco, Xiaoyu Piao, Shana Massar, Anton Potocnik, Kristiaan De Greve – IMEC
Superconducting Nb airbridges were fabricated in imec's 300 mm pilot line utilizing an advanced production toolset. An optimized process flow, which does not rely on liftoff or shadow evaporation, results in high airbridge yield across full wafers, and is compatible with trilayer-based superconducting qubit fabrication methods. Airbridges integrated with resonators were characterized at millikelvin temperatures, showing that the addition of airbridges has minimal contribution to microwave losses. This work demonstrates that airbridges can be incorporated into foundry compatible qubit fabrication flows.

3:30 – 3:50 Coffee Break

Session 9: DTCO & Advanced Interconnects III
Chair: Susumu Matsumoto (Tower Partners Semiconductor) & Nick Lanzillo (IBM Research)

3:50 – 4:20

9.1 What Role Could 2D Materials Play in the Semiconductor Industry? (Invited)

Eric Pop – Stanford University

4:20 – 4:40

9.2 A design approach for ultra-low-k dielectric organosiloxane polymers

Hanna Melissa Luusua, Thomas Gädda, Jagadish Salunke, Zhongmei Han, Heli Kekkonen, Juha Rantala, Hsiaokang Chang, Hsin-Yen Huang, Ting-Ya Lo, Gary Li – PiBond Oy, Taiwan Semiconductor Manufacturing Company

Capacitance reduction is crucial for advanced interconnect scaling. Decreasing dielectric constant of inter layer dielectric (ILD) and inter metal dielectric (IMD) contributes significantly to the decrease of capacitance. Spin-on organosiloxane polymers have many advantages as ILD and IMD materials, including high thermal stability, easy processing, and dielectric constant (k) lower than 3. For further k reduction, introduction of porosity is the most common strategy to achieve k< 2.7. However, highly porous materials can suffer from e.g. poor mechanical properties, resulting in several integration challenges. We have demonstrated a material design approach for low-k organosiloxane dielectric polymers, enabling ultra-low-k (<2.5) spin-on thin films without introducing porosity to material.

4:40 – 5:00

9.3 Investigation of Graphene Cap Formation on NiAl by Low Temperature Thermal CVD *(Student Paper)*

Yumehito Temmyo, Jean-Philippe Soulie, Christophe Adelmann, Zsolt Tokei, Kazuyoshi Ueno – Shibaura Institute of Technology, IMEC

In order to suppress the increase in resistivity due to surface oxidation of NiAl thin films, we developed a process for forming a graphene cap on the NiAl surface with using an ultra-thin Ni layer and the optimized thermal CVD at 400 °C. Although Ar-plasma cleaning of NiAl surface was found to promote the CVD reaction at the surface, CNT-like features were formed due to non-uniform Ni on the NiAl surface. A 2 nm Ni layer on NiAl can promote a uniform deposition of carbon film with the optimized CVD condition of lower thermal budget and higher precursor supply. There was no increase in the resistivity of optimized C/Ni/NiAl film during annealing in the air up to 400°C.

Poster Session and Conference Reception (5:30 – 8:00)

Posters
Chairs: Fumihiro Inoue (Yokohama National University) & Chris Wilson (IMEC)

P1. Redefining 2-Level Semi-Damascene Interconnect Technology: Benchmarking three different Fully Self-aligned Via options

Giulio Marti, Gilles Delie, Gayle Murdoch, Anshul Gupta, Souvik Kundu, Stefan Decoster, Olalla Varela Pedreira, Alicja Lesniewska, Yannick Hermans, Bart Kenens, Fulya Ulu Okudur, Seongho Park, Zsolt Tokei – IMEC

This study highlights the effectiveness of a novel two-metal-level semi-damascene integration approach using fully self-aligned pillar-vias (FSAV) for interconnects ranging from 18 to 26 nm metal pitch. We employ EUV-SADP-SIM patterning scheme and direct metal etch of Ru to demonstrate the proof of concept on 300 mm wafers on 300mm wafers. This integration not only gives lower via resistance than the previously reported schemes but also promise lowers capacitance between the two metal layers. Furthermore, it significantly widens the via litho and etch process window, making it more attractive for advanced semiconductor manufacturing.

P2. Self-aligned 8nm T2T as cell boundary in the middle-of-line

Philippe Marien, Yannick Hermans, Subhobroto Choudhury, Souvik Kundu, Stefan Decoster, Fulya Ulu Okudur, Naveen Reddy, Bart Kenens, Nicolas Jourdan, Gilles Delie, Giulio Marti, Chen Wu, Victor Vega Gonzalez, Gayle Murdoch, Seongho Park, Zsolt Tokei – IMEC

In order to achieve tight, 8 to 12 nm cell boundaries, Ru direct metal etch can be used to split a larger via into two opposite facing smaller vias and create a tight metal line tip-to-tip (T2T) at the cell boundary. This is obtained by self-aligning the Ru direct metal etch to the tightest metal layer above. This technique of splitting a via and creating a T2T with zero line extension is promising for cell boundary definition of complementary FET. In this work, we will discuss lithography overlay and via CD process window definition to achieve the improved morphological and electrical results. For 8 nm T2T, we have obtained a 55% leakage current yield. Additionally, for 10 and 12 nm T2T, a leakage current yield of above 90% was achieved.

P3. Demonstration of MP18-26nm Ru Semi-Damascene Spacer-is-Dielectric SADP Integration

Chen Wu, Stefan Decoster, Vincent Renaud, Yannick Hermans, Philippe Marien, Giulio Marti, Nancy Heylen, Bart Kenens, Syamashree Roy, Fulya Ulu Okudur, Quoc Toan Le, Naveen Reddy, Alfonso Sepulveda Marquez, Gilles Delie, Anshul Gupta, Alicja Lesniewska, Gayle Murdoch, Seongho Park, Zsolt Tőkei – IMEC

This work presents a novel Spacer-is-Dielectric (SID) SADP Ru semi-damascene integration scheme by using metal-based core and gap hard masks. More than 70% yield in tested line resistance and line-to-line leakage, especially in MP18 structures, confirm the flow feasibility. The tested MP18 structures show a median line resistance of 720 Ω/μm and a clean line-to-line leakage with breakdown voltages in the range of 12-14V.

P4. Technology benchmarking of copper electromigration using a grain-sensitive simulation framework *(Student Paper)*

Ahmed S. Saleh, Kristof Croes, Hajdin Ceric, Ingrid De Wolf, Houman Zahedmanesh – IMEC

A calibrated simulation framework for the analysis of electromigration (EM) in nano-interconnects, incorporating the intricate influence of microstructure, is presented. Different technology options were benchmarked for EM performance, taking copper texture and microstructural changes with scaling into account. Specifically, the impacts of metal cap and copper doping were simulated for a constant line height of 80nm and for linewidths between 20 and 100nm. An almost linear increase in normalized lifetime was observed for aspect ratios of 1 and above. An increase ranging from 10x to 100x was gained by using a metal cap for aspect ratios below 2. However, its effectiveness strongly weakened with decreasing CD with almost no EM lifetime gain for 20nm CD. Doping elements that lower grain boundary diffusivity were found to be more effective at these small dimensions.

P5. Patterning process and electrical yield optimization at the limits of single exposure EUV 0.33 NA: a pitch 26nm damascene process

Victor M. Blanco Carballo, Kevin Vandersmissen, Bart de Wachter, Kathleen Nafus, Yannick Feurprier, Thiam arame, Alex Hsu, Cyrus Tabery, Jan Doise, Peter De Schepper – IMEC, TEL, ASML, Inpria

In this work we have developed a single layer short loop damascene process to evaluate and optimize patterning performance of pitch 26nm single exposure 0.33 NA EUV. An electrical readout of 1m long meanders and forks-forks is used to compare the different processes and evaluate the amount of resist defects leading to shorts or opens. For the best process a full wafer combo yield of 99.7% is achieved (edge excluded) equivalent to 12 defects/cm2

P6. Interconnect Delay Modeling of Critical Paths in Angstrom Nodes *(Student Paper)*

Francesco Dell'Atti, Anita Farokhnejad, Odysseas Zografos, Pieter Weckx, Julien Ryckaert, Paul Heremans – IMEC

This work provides a methodology to analyze and model critical path interconnections of physically implemented digital designs in Angstrom nodes. The Elmore delay computation is applied to the detailed interconnect topology to provide a block-level statistical assessment of dominant parameters such as wire and via resistance (R), as well as wire and pin capacitance (C), on interconnect performance. Our methodology can rapidly assess the impact of back-end-of-line (BEOL) materials, interconnect geometries, and scaling boosters on the interconnect delay of complex digital designs, enabling fast turn-around time for Design-Technology Co-optimization (DTCO) loops. The model predicts delays with 1.3 percent of maximum mean error, standard deviations below 3 percent, and 23x speedups compared to conventional Static-Timing-Analysis (STA) sensitivity analyses.

P7. Ion Beam Deposition of Low-Resistivity Tungsten and Molybdenum for Interconnect Applications

Rutvik Mehta, Yuejing (Crystal) Wang, Ashish Kulkarni, Robert Walko, Paul Turner, Frank Cerio, Robert Caldwell – Veeco Instruments, Inc.

Refractory metals like tungsten and molybdenum with favorable resistivity scaling effects are promising candidates for nanometer scale interconnects for memory and logic. Ion beam

deposition with the highest sputter energy and fine-scale control of deposition energetics enables metal thin films with ideal microstructures. Tungsten and molybdenum thin films deposited by ion beam deposition on 300mm wafers show large grained fully (110)-aligned microstructures presaging low-resistivity independent of the underlying substrates. Unlike other deposition approaches which require additional inserted layers and show underlayer dependence, ion beam deposition achieves lower resistivity in the as-deposited state independent of the underlying substrate. Resistivity versus thickness curves of ion beam deposited tungsten and molybdenum films shows ultra-low resistivity in the as-deposited state with scaling effects qualitatively similar to that of corresponding epitaxial films. These results establish the application of ion beam deposition of refractory metals as a very promising approach towards low-resistivity interconnects for the next generation of integrated devices.

P8. Formation of Lateral-Type High-Tc Superconductor Josephson Junction by Helium Ion Microscopy

Shinichi Ogawa, Tetsuro Misawa, Kosuke Kurushima, Yuji Otsuka, Yukinori Moritta, Chiharu Urano – National Institute of Advanced Industrial Science and Technology, Toray Research Center, Inc.

This paper presents, for the first time, the results of investigating the dependence of ion dose and temperature on the formation of Josephson junctions via helium ion irradiation of YBa2Cu3O7-δ; high-temperature superconductor thin films. Helium ion microscopy technology was employed for the helium ion irradiation. Our observations reveal that the characteristics of Josephson junctions can be controlled by the dose of helium ions. Converging the helium ion beam to a diameter of 0.35 nm, with an acceleration voltage of 30 kV, and an irradiation dose in the order of 1E17/cm2, demonstrates the formation of excellent lateral-type thin film Josephson junctions.

P9. Selective Co ALD for Chiplet-to-Wafer and Wafer-to-Wafer Bonding *(Student Paper)*

Cheng Hsuan Kuo, Madison Manley, Dipayan Pal, Rohan Sahay, Ravi Kanjolia, Mansour Moinpour, Jacob Woodruff, Jeffrey Spiegelman, Muhannad Bakir, Andrew Kummel – UCSD, Georgia Institute of Technology, EMD Electronics, RASIRC

Cyclic clean treatment by using strong oxidant: HOOH and reductant: N2H4 ¬was developed for Cu cleaning which can be applied in the inverse hybrid metal bonding process. Compared to UHV anneal at higher temperature (415C), cyclic clean process is only performed at 340C with lower surface impurities. Also, highly selective Co ALD is deposited on metal Cu but not on SiO2 even after 1000 ALD cycles.

P10. Enhancement of electromigration performance of molybdenum nanowires by CoMo capping

Sijie Gu, Haijun Cheng, Chun-Feng Hu, Xin-Ping Qu Ping – Fudan University

The electromigration performance of the Mo nanowires with different capping layers is measured. Results show that the CoMo capped Mo nanowires show better electromigration performance than that of the ones capped with Si3N4 or SiO2. It is found that the CoMo capping layer can effectively protect the Mo film from oxidation as well as nitridation, which is the main reason for the improved EM performance of the Mo nanowires.

P11. Data Analytics to Identify Improved Low k Films

William Entley, Achtyl Jennifer, Robert Ridgeway – EMD Electronics

This paper investigates the development of as deposited dense low k films with high mechanical strength, crucial for advanced semiconductor manufacturing. Over 1100 unique low k films from seventeen precursors were deposited and analyzed, focusing on mechanical properties. The study used a Design of Experiments (DOE) approach to maximize mechanical strength of each precursor. Data analytics were used to analyze and sort the low k films to identify precursors that had the highest mechanical strength at a given value of the dielectric constant. This was done by extracting the Pareto Frontier, representing films with the highest mechanical strength at varying dielectric constants, for each precursor. Results showed significant variation in mechanical strength among precursors, with two novel precursors exhibiting superior performance compared to DMDMOS, an industry standard precursor. Analysis of the carbon distribution in the films provided insight into mechanical strength variations. This research highlights the potential of tailored precursor design to meet the demanding requirements of dense low k films in advanced semiconductor nodes.

P12. Halogen Free Low Temperature ALD Mo-based Films for Interconnects Applications

Aein Babadi, Randall Higuchi, Mike Savo, Charlene Chen, Bhushan Zope, Sergei Ivanov – EMD Electronics

Molybdenum-based films synthesized by low temperature atomic layer deposition (ALD) from different organometallic halogen free Molybdenum precursors. The film s average composition was investigated and correlated with their nanoscale structures and electrical transport properties. A high work function N-rich MoN film with low carbon contamination was demonstrated in comparison with MoC/MoCN films with low resistivity. The precursor composition dependence of film's properties leads to a low resistivity MoC film as well as selective deposition of Mo films on metallic substrates.

P13. Surface Characterization and Modification for Cu/SiCN Hybrid Bonding

Kenta Hayama, Kohei Nakayama, Ryosuke Sato, Yutetsu Kamiya, Ken Harada, Masahiro Yokoyama, Yasuhiro Kawase, Fumihiro Inoue – Yokohama National University, Mitsubishi Chemical Corporation

Hybrid bonding is an ideal bonding scheme for achieving finer interconnect pitch in multiple applications. To ensure high yielding, the pre-bonding surface preparation is a crucial process step as hybrid bonding requires surface uniformity of Cu pad. In this study, the influence of P-CMP cleaning and the effect of N2 plasma activation on Cu pad were investigated. The P-CMP alkaline cleaning solution can remove BTA residues. Furthermore, the plasma activation turns the Cu surface without any carbon related residues even with 15 sec process time. These results suggest an optimized surface condition for fine-pitch hybrid bonding.

P14. Low contact resistance copper-copper bonding with selective electroless plating cobalt interlayer

Yun-Hao Shao, Zihong Ni, Gui Chen, Hao Wang, Xin-Ping Qu – Fudan university

Low temperature metal direct bonding is very challenging in 3D interconnect technical. In this work, self aligned Co layer is selectively deposited on the copper line by electroless plating as an interlayer for Cu-Cu bonding. The direct bonding between Cu/Co is performed without a chemical mechanical polishing process at 250°C; in ambient. An intact bonding interface is observed and a specific contact resistance of $5.5\times10^{-7}\ \Omega\cdot cm^2$ is obtained. Through a special surface treatment, the specific contact resistance can achieve $3.8\times10^{-8}\ \Omega\cdot cm^2$, which is lower than that of Cu-Cu bonding with PVD Co interlayer.

P15. Cyclic Etching of Mo Nanowires

Ivan Erofeev, Antony Winata Hartanto, Harold Philipsen, Antoine Pacco, Muhaimin Mareum Khan, Zainul Aabdin, Frank Holsteyns, Utkur Mirsaidov – National University of Singapore, IMEC

We show that a uniform recess of polycrystalline Mo films and nanowires can be achieved using a cyclical two-step method: isotropic oxygen plasma-based surface oxidation followed by selective etching of this oxide layer. The oxidation step fully defines the recess depth, and the low facet dependence of plasma oxidation ensures its uniformity. Our study describes the parameters (RF power, gas pressure, and exposure time) that affect and control the uniformity of oxidation of patterned Mo nanowires. We showed that using highly selective oxide etching, we can perform multiple etching cycles with a typical etch rate of 1-2 nm per cycle, depending on the RF power. Due to plasma isotropy, this approach can be implemented for a controlled uniform etching of large vertical stacks of metal nanostructures.

P16. Characterization of Siliconcarbonitride bonding layer for plasma activated direct fusion bonding

David Doppelbauer, Christoph Floetgen, Ignacio Gabriel Vicente Gabàs, Serena Iacovo, Steven Brems, Eric Beyne, Jiri Duchoslav, Heiko Groiss – EV Group E. Thallner GmbH, IMEC, Johannes Kepler University Linz

In the scope of this work, a comprehensive study of plasma treated Silicon carbonitride (SiCN) dielectric bonding surfaces on Si wafers is presented. PECVD grown films were investigated by means of variable angle spectroscopic ellipsometry (VASE) and angle-resolved x-ray photoelectron spectroscopy (ARXPS) before and after plasma activation. Based on ARXPS depth-profiling data, an ellipsometry model was developed, allowing for non-destructive characterization of the plasma effect on the SiCN bonding surfaces. Oxidation processes and intermediate mixture phase layers between the grown oxide and the SiCN layer were observed and correlated to plasma specific characteristics as measured by current-voltage probes. The plasma activation effect was further evaluated after bonding of SiCN wafer pairs in terms of bonding energy. Plasma characteristic parameters correlate well with oxide thickness after plasma activation and bonding energy.

P17. Investigation of the enlargement of Ru grains and failure modes analysis in microsecond UV laser annealing

Zeinab Chehadi, Richard Daubriac, Lu Lu, Karim Huet, Zsolt Tokei, Leonardo Cancellara, Fuccio Cristiano, Louis Thuries– LASSE-Screen, LAAS-CNRS, ScreenSPE, IMEC

Interconnects based on Ru has been considered as a promising candidate to replace Cu-based interconnects for the future technology nodes thanks to its low bulk resistivity , its short electron

mean free path (e-MFP) and the possibility to have a barrier-less integration. In this work, we demonstrate that µs UV Laser Annealing (UV- LA) is an interesting process strategy to reduce the metal line resistance by enlarging grains in thin Ru films. A method based on numerical simulations has been proposed to optimize the LA conditions to lower the Ru film resistivity close to the bulk one, while avoiding the apparition of structural damages such as wrinkles or buckling.

P18. Nano-chemical characterization of SiO2 and Cu surfaces for Cu-Cu hybrid bonding

Padraic O'Reilly, Beihang Yu, Cheng Hsuan Kuo, Andrew Kummel, Ricardo Ruiz, Sung I. Park – Molecular Vista, Inc., Lawrence Berkeley National Laboratory, UCSD

Infrared photo-induced force microscopy (IR PiFM), which combines non-contact atomic force microscopy and infrared spectroscopy (AFM IR), is applied to precisely characterize the surface chemical state of the silicon oxide and copper. Based on an AFM platform, the technique can monitor the topographical condition (flatness of the dielectric as well as the recession of the Cu pads) in addition to the surface chemistry (absence of unwanted molecules and the presence of desired surface termination), both with ~ 5 nm lateral resolution and monolayer sensitivity, to characterize the suitability of the samples for successful Cu-Cu hybrid bonding.

P19. 300mm Wafer-scale ALD-grown MoS2 for Cu diffusion barrier

Thong Ngo, Angelica Zacatzi, Yuanqiu Tan, Daniel Lee, Anand Wankis, Nguyen Vu, Ravi Kanjolia, Mansour Moinpour, Zhihong Chen – EMD Electronics, Purdue University

Cu has served as the interconnect metal in various chip generations, typically accompanied by a TaN/Ta diffusion barrier/liner. The size-scaling demand for future nodes requires thinning down TaN/Ta bi-layer. The thickness of TaN/Ta has reached the limit of its barrier/liner capability, necessitating the exploration of alternative diffusion barrier/liner materials. In this paper, we report the 300mm wafer-scale atomic layer deposited MoS2 as a promising candidate for Cu diffusion barrier/liner interconnect. MoS2 was deposited on thermal SiO2 substrate at the temperatures ranging from 200-550 °C. Good conformality of MoS2 was demonstrated on high aspect ratio structure. The resistivity of Cu/MoS2/SiO2 stack is lower than that of Cu/SiO2 stack. Time dependent dielectric breakdown of Cu/MoS2/SiO2 will be discussed and benchmarked with Cu/Ta/TaN/SiO2.

P20. Investigation of the Low Dielectric Constant Properties of SiOx/AlOx Nanolaminate Film *(Student Paper)*

Xinyu Wang, Jing Mu, James Huang, Yunil Cho, Kesong Wang, Dipayan Pal, Ajay Yadav, T. Wong Keith, Ellie Yieh, Srinivas Nemani, Andrew Kummel – UC San Diego, Applied Materials

Low-k materials play a pivotal role in semiconductor technologies, primarily due to their capability to enhance signal transmission speed and reduce power consumption. This study investigates a series of novel low-k (<2.5) SiOx/AlOx nanolaminate films with smooth surfaces deposited on Si substrates via a dual-temperature thermal chemical vapor deposition (CVD) process. The low dielectric constant value achieved by the nanolaminate is ascribed to its porous nature. Additionally, incorporating carbon into the nanolaminate structure greatly enhanced the atmospheric stability of the film by making it hydrophobic.

P21. Enhanced process control for plasma triggered oxide growth in plasma activated wafer bonding

Christoph Floetgen, Ignacio Gabriel Vicente Gabàs, David Doppelbauer – EV Group E. Thallner GmbH

In Plasma Activated Wafer Bonding (PAWB) the plasma process modifies the surface conditions of a substrate, allowing for low-temperature annealing of the wafers to be bonded. Despite its critical role in the PAWB process, plasma treatment is often insufficiently characterized. In this study, electrical plasma parameters are recorded during the plasma activation process using current-voltage probes at the plasma chamber electrodes. These parameters are then correlated with bonding quality metrics like the plasma-triggered oxide growth on Si and the bond strength after annealing. As will be shown, particularly the oxide thickness grown after plasma activation can be determined by a simple functional correlation to plasma characteristic electrical parameters connected to the total dose of ions impinging on the wafer surface. This allows for potential enhanced process control, specifically in the light of the industry's current and future challenges of shrinking device nodes.

P22. Metal-metal contact resistance measurements

Poyen Shen, Daniel Gall – Rensselaer Polytechnic Institute

The contact resistance at metal-metal (W, Mo, Ru, Co, TiN) interfaces is determined using a new method based on blanket superlattice thin films where the resistivity ρ parallel to the interfaces is measured as a function of superlattice period Λ to quantify the electron interface scattering. Epitaxial W(001)/Mo(001) superlattices show a continuous resistivity increase from 7.10 to 8.62 μΩ-cm with decreasing Λ = 50-1.7 nm, indicating a contact resistance of 2.6×10-16 Ω-m2. Ru/Co multilayers show a much more pronounced increase from 15.0 to 47.5 μΩ-cm with Λ = 60-2 nm which is attributed to atomic intermixing leading to an interfacial Ru-Co alloy with a high measured ρ = 61 μΩ-cm and a Ru-Co contact resistance for interfaces deposited at 400 °C of 9.1 $\times 10^{-15}$ Ω-m2. Ru/TiN and Co/TiN interface resistances are dominated by the high ρ for TiN, and are therefore proportional to the TiN thickness.

P23. Wafer-Level Electrochemical Deposition and Processing of Nanotwinned Cu RDL

Chih-Hao Hsia, SungHo Park, Soichi Watanabe, Marco Arnold, Zaid El-Mekki, Martine Delande, Ehsan Shafahian, Punith Kumar M. K. Gowda, Herbert Struyf, Aleksandar Radisic – BASF, IMEC

We have successfully performed wafer-level (300 mm) fabrication of highly (111) oriented nanotwinned copper (nt-Cu) Redistribution layers (RDL) using through-resist electrochemical deposition on barrier/seed combinations such as TiW/Cu, TaN/Cu, and TaN/Ta/Cu. We have examined physical-chemical properties of nt-Cu and explored possible challenges in post-plating processing of these structures. After photoresist removal, nt-Cu lines were analyzed using Scanning electron microscopy (SEM) and Focused ion beam (FIB) techniques. Within wafer (WIW) and within die (WID) feature height uniformity were measured using profilometry and Cu losses in the plated lines upon wet-etch of the Cu seed were examined using automated SEM measurements.

P24. Mechanistic and Performance Aspects for Co-designed Process Technology to Enable Mo as the Next Generation Conductor

Michael White, Kevin Dockery, Paul Besser, Daniela White, Bryan Hendrix, Don Frye, Maryam Farmand, Jun Liu, Das Atanu, Jason Seabold, Fernando Hung – Entegris

PVD and CVD molybdenum (Mo) wafers/coupons were prepared and analyzed by various techniques including XPS, electrochemistry, impedance spectroscopy, AFM, Zeta Potential, Raman as well as ATR FTIR spectroscopies. The surface chemistry was then correlated with performance parameters such as the static etch and polishing rates/profile in addition to the defectivity after Planarcore® brush cleaning using with Entegris ML slurries and AG-Mo series PCMP cleaners.

P25. The investigation of Ar plasma treatment on the contact resistance between metal-metal by a simple metal bonding simulation approach

Gui Chen, Yun-Hao Shao, Xin-Ping Qu – Fudan University

Reducing the direct metal bonding temperature is a challenge for 3D metal bonding. We present a simple fabrication process using the two-step PVD Cu / Co on the PVD Co / Cu surface with a vacuum break followed by annealing to simulate the real metal-metal bonding. Based on this approach, without critical requirement of cleanliness of the bonding surface, the parameters which impacts the bonding temperature and interface specific contact resistance can be efficiently find out. In this work, we first used this approach to choose the correct Kevin structure to measure the low contact resistance, and then the effects of Argon plasma activation of the Co layer, which is used as an interlayer for Cu-Cu bonding, were investigated. It is found that the Ar plasma activation can result in uniform Co3O4 layer formation and effectively reduce contact resistance.

P26. Doping Effects in Grain Boundaries of Tungsten: Insights from First-Principle Study

Yeongjun Lim, Mincheol Shin – Korea Advanced Institute of Science and Technology

As semiconductor device sizes shrink to the nanometer scale, the sharp increase in resistance due to grain boundary and surface scattering poses uncertainties regarding the continued use of copper as an interconnect material. In pursuit of alternatives, tungsten has emerged, but its high resistance due to scattering remains a challenge. This study investigates the effects of grain boundary doping, a potential method for reducing resistance, through first-principle simulations combining density functional theory (DFT) and non-equilibrium Green's function (NEGF) method. Our simulations reveal that grain boundary doping with certain impurities can effectively reduce resistivity in specific coincidence site lattice grain boundaries of tungsten interconnects.

P27. The feasibility of the lateral wet-etching on TiN layers in 3D multilayer stack structure

Jiao Jin, Jiabao Sun, tuo xin, Weidu Qin, Chaoyang Guan, wenjun chen, Chao Tian, Baodong Han, Hongbo Sun, Chao Zhao – Beijing Superstring Academy of Memory Technology

3D Memory Device is manufactured based on dielectric materials of SiOx and SiN vertically multilayer stacked semiconductor structures. Atomic Layer Deposition (ALD) have homogeneous step coverage of sidewalls and bottom with high aspect ratios in achieve 3D structure. But existing inherently void defect in lateral pocket layers. The worse uniformity and profile appeared after wet lateral etch along with pre-process layer seam, affecting seriously the storage

properties of the device and lead to slower transfer speeds. In this study, Oxide Trim (wet isotropic etching SiOx) provides a new strategy for wet lateral etching TiN thin films by ALD technology of seam issue. The trumpet shaped opening between the stacked layers formed by twice lateral wet etching SiN promoted the seam inward after deposition, potential increasing the filler metal density in the seal and improving the BL uniformity using wet chemical of high etching selectivity for TiN to SiOx/SiN.

P28. Proposal for Improved Electrical Efficiency through Thermal Modeling of Interconnect Structure *(Student Paper)*

Taeyeong Hong, Seul Ki Hong – Seoul National University of Science & Technology

This study investigated the modeling of heat and current distribution in interconnect structure used in semiconductor systems based on their shapes, utilizing Finite Element Method (FEM) simulations. The research aims to optimize power efficiency in interconnect structures by securing the modeling of heat and current distribution through experimental validation, confirming the integrity of the models. In interconnect structures, the current density increases as the contact area for current flow at the junction of metal lines and vias narrows, leading to a temperature rise due to Joule heating. The need for scaling down exacerbates the issue as the dimensions need to be progressively reduced, conforming to the specifications of both lower and upper components, causing a reduction in the width of the conductors. The temperature increase due to Joule heating is inevitable with this reduced area, and it ultimately leads to the destruction, directly impacting the reliability of the entire system. The experimental results provide considerations for reliability when significantly scaling down interconnect structures in current semiconductor systems. Furthermore, these findings can be widely applied to research aimed at developing interconnect structures that enhance reliability.

P29. Lateral Metal Deposition and the Formation of Interconnection

Weidu Qin, Jiabao Sun, Jiao Jin, Chao Tian, Chaoyang Guan, Hongbo Sun, Chao Zhao – Beijing Superstring Academy of Memory Technology

With the development of semiconductor technology, the device architecture has developed from two-dimensional stacking to three-dimensional stacking, which makes it difficult to deposit interconnected metal films in multi-layer stacking structures. In order to obtain higher quality interconnection films, we used atomic layer deposition (ALD) and WET ETCH process to form TiN metal films in a multilayer stacked lateral structure. After WET ETCH, a straight profile was obtained and a seam-control TiN film was formed. This method shows good potential in depositing high-quality thin films and forming metal interconnections in multi-layer stacked devices.

P30. Thermally Conductivity Study of One Micron AlN Deposition by Bipolar High Power Impulse Magnetron Sputtering *(Student Paper)*

Ping Che Lee, Mcleod Aaron, Mingeun Choi, Vaca Diego, Satish Kumar, Andrew Kummel – UCSD, Georgia Institute of Technology

High Power Impulse Magnetron Sputtering (HIPIMS) has emerged as a promising technique for the deposition of thin films with superior properties. In this study, HIPIMS was combined with a

positive target bias (Kick voltage) process to enhance AlN film quality further. Aluminum Nitride (AlN) thin films were deposited using this method and characterized using Transmission Electron Microscopy (TEM) and X-Ray Diffraction (XRD). The thermal properties of the films were investigated using Frequency Domain Thermoreflectance (FDTR). The results show that the HIPIMS plus Kick process significantly improves the film quality, leading to enhanced thermal conductivity (112 W/ m·K) compared to conventional techniques. This work demonstrates the potential of HIPIMS in producing high-quality thin films with improved thermal properties, making it suitable for various applications in electronics and thermal management.

THURSDAY, JUNE 6, 2024

Session 10: Keynote
Chair: Zhihong Chen

8:15 – 9:05
Keynote – Memory Technology: Status and Scaling Perspective
Dr. Nirmal Ramaswamy – Micron

Session 11: 3D Packaging & Integration
Chair: Arup Saha (ASML) & Harsono Simka (Samsung)

9:05 – 9:35
11.1 High Performance 3D Flash Memory based on CBA (CMOS Directly Bonded to Array) Technology (Invited)
Shigeki Kobayashi – Kioxia

9:35 – 10:05
11.2 Reconfigured Wafer-to-Wafer 3D Integration with Meta Bonding Technologies (Invited)
Takafumi Fukushima – Tohuku University
Reconfigured Wafer-to-Wafer (RWoW) 3D integration represents the pinnacle of this process. RWoW is an advanced multi-chip-to-wafer 3D integration method that employs self-assembly with liquid droplets. The critical steps involve temporary bonding to carrier wafers and the transfer of multiple chips from these carrier wafers to target wafers. Fukushima *et al*. have termed carrier wafers with self-assembled known good dies (KGDs) as “Reconfigured Wafers.” Initially, various 1st-layer KGDs equipped with microbumps are sorted from different device wafers post-testing. These KGDs are then self-assembled on a carrier wafer and temporarily bonded in a face-down manner. Subsequently, the carrier wafers are aligned and bonded to the respective target interposer or IC device wafers, which feature an identical microbump design to the self-assembled KGDs. Similar innovative technologies, such as “Collective Bonding” and “Reconstructed Wafers” have appeared later.

The bonding between KGDs and target wafers employs microbump-to-microbump bonding or direct/hybrid bonding, followed by detachment of the KGDs from the carrier wafers and their transfer to the target wafers. The ensuing steps include underfilling and multi-chip thinning, encompassing backside grinding/CMP and TSV/microbump formation. The final stage involves vertically stacking these KGDs in layers by repeating the multi-chip transfer processes. We call the advanced chip/wafer bonding technology "Meta Bonding" such as fine-pitch microbump bonding, ultrafine-pitch hybrid bonding, and DSA bonding and more. for coming future high-performance and multi-functional 3D and heterogeneous holistic systems including BSPDN, C-FET (Complementary Field-Effect Transistor), and Photonic/Quantum/DNA/Molecular IC etc.)

10:05 – 10:35

11.3 3D Stacking Technology Challenges for High Bandwidth Memory (HBM) (Invited)

Ho Young Son – SK Hynix Semiconductor

10:35 – 10:55

11.4 Study and Control of the Distortion Induced by the Bonding Process for BSPDN Approaches

Karine Abadie, Ivanie Mendes, Marie-Line Pourteau, Fournel Frank, Hadi Hijazi, Balan Viorel, Richard Van Haren, Suwen Li, Blandine Minghetti, Leon Van Dijk, Mart Baars, Laurent Michaud, Thomas Plach, Gernot Probst – Université Grenoble Alpes, CEA-leti, ASML, EV Group

With the development of the Back-Side Power Delivery Network (BSPDN), new challenges and specifications in terms of alignment for subsequent exposure steps arise. Indeed, for 2-nm node technology this requires a very fine correction of the distortion induced by all the process steps on the transferred thin layer. One process step in particular seems to have a predominant effect on this aspect: the bonding. This paper introduces the methodology developed at CEA-Leti in collaboration with ASML and EV Group, to characterize the distortion induced by the direct bonding process step at global and local scale. The integration flow simulates BSPDN approach, considering a thin silicon layer to be transferred to another substrate, and allows developing innovative immersion scanner correction strategies.

10:55 – 11:15

11.5 Bonding induced distortion in wafer-to-wafer bonding applications: how the scanner and Yieldstar can enable 3D integration

Victor M. Blanco Carballo, Vincent Renaud, Serena Iacovo, Anne Jourdain, Alex Hsu, Yun-Heng Tseng, Cyrus Tabery, Etienne De Poortere – IMEC, ASML

In this work, we have developed a two-layer short loop process on device wafers to study the distortion fingerprint induced by a wafer-to-wafer bonding process. The alignment grid is used to characterize the after-bonding wafer deformation. Alignment modeling and optimization was performed to reduce the expected backside process overlay to below 5nm as well as the wafer-to-wafer variability.

11:15 – 11:35 Coffee Break

Session 12: Materials & Unit Process III
Chairs: Tom Mountsier (LAM Research) & Mansour Moinpour (EMD Electronics)

11:35 – 11:55

12.1 Low Resistance Stacked Via Metallization for Future Interconnects

Marleen H. van der Veen, Anita Farokhnejad, Akhilesh Kumar Mandal, Herbert Struyf, Seongho Park, Zsolt Tőkei – IMEC

We present stacked via and wire resistance predictions to find low resistive via metallization schemes that improve the system performance for sub-2 nm nodes. Implementing Ru vias with Cu wires at EUV patterned levels can give up to 60% resistance reduction. The circuit benefit of using Ru vias is determined with enhanced ring oscillator (RO) simulations. The Ru-Cu hybrid metallization in V2-M5 EUV printed layers gives a 10% frequency improvement as compared to stacks with semi damascene (SD) Ru and dual damascene (DD) Cu. The implementation of the selective Ru on Cu is demonstrated in metal pitch (MP) MP21-MP24 DD structures with yielding chains and vias that meet their resistance target.

11:55 – 12:15

12.2 Selective CVD Ru on W by sequential small molecule inhibitor treatments

Kai-Hung Yu, Ryota yonezawa, Hirokazu Aizawa, Wajda Cory, kawasaki Hiroaki, Mayersky Joshua, Suzuki Hidenao – TEL Technology Center, America, LLC

This paper presents a method of sequential surface treatments that effectively extends the selectivity of metal deposition onto desired metal surfaces and suppresses undesired nuclei defects. Two different types of Small Molecule Inhibitors (SMIs) were used in this paper to demonstrate that Chemical Vapor Deposition CVD Ruthenium can be deposited on W metal surface selective to SiO2 dielectric surface. A Chemical Mechanical Planarization (CMP) process exposed both W and SiO2 on top of patterned surfaces which was then used for testing the concept of Area Selective Deposition (ASD). Whole wafer In-Line electrical Test (ILT) results were used to demonstrate the selectivity loss. Undesired nuclei defects on the SiO2 surface correspond to an increase in the measured leakage current.

12:15 – 12:35

12.3 Dielectric Relaxation in HfO2/Al2O3 MIM Capacitors

Jeff Gambino, Vincent McGahay, Gyana Biswal, Akihiro Hasegawa, Michael Cook, Thomas Long, Karen Barker, David Price, Rick Mauritzson – Onsemi

Dielectric relaxation has been measured in HfO2/Al2O3 MIM capacitors. The dielectric relaxation current exhibits a weak temperature dependence, with activation energies ranging from ~ 0.067 eV (20 msec after voltage pulse) to ~0.15 eV (2 sec after voltage pulse). It is proposed that the initial dielectric relaxation is from electron emission from shallow traps, whereas the later dielectric relaxation is from emission from deep traps.

12:35 – 1:50 Lunch

Session 13: DTCO & Advanced Interconnects II
Chair: Chris Wilson (IMEC)

1:50 – 2:20

13.1 Materials for switchable interconnects, ferroelectrics/IWO

Suman Datta – Georgia Tech

2:20 – 2:50

13.2 Towards a comprehensive solution for future interconnects

Gert Leusiak – TEL

2:50 – 3:10

13.3 Ligand Engineering to Machine learning: Optimizing Ru ALD for Ultrathin Film Deposition

Jay Chiu, Isiah Liu, Chang-Won Lee, Guo Liu, Bhushan Zope – EMD Electronics, a business of Merck KGaA, Darmstadt

This study demonstrated our significant advancements in H2-based thermal Ru ALD, using novel Ru precursors, RuEM8 and RuEM10, which enable fabrication of ultra-thin Ru films with: excellent continuity at thicknesses as low as 3 nm, over 99% conformality, greater than 99 wt.% purity, and bulk resistivity reduced to 15 uΩ·cm. Such attributes position them as prime candidates for interconnect applications. Those breakthroughs were built on our strategic innovations: (1) A Machine-learning guided DoE methodology for high-efficiency ALD process optimization. (2) Smoothing-agent post-treatment to improve continuity via modulating Ru surface diffusion. (3) tailored ligands as in-situ inhibitors to facilitate 2D Ru growth. This showcased the combination of chemistry domain knowledge and machine learning forms the basis of a high-efficiency ALD precursor development methodology.

3:10 – 3:30

13.4 Modeling of Via Resistance considering Spatially-Resolved Conductivity and Temperature-Dependence *(Student Paper)*

Xinkang Chen, Sumeet Gupta – Purdue University

This paper presents a physics-based via resistance model featuring spatially-resolved conductivity due to surface scattering based on the Fuchs-Sondheimer (FS) theory, grain boundary scattering based on Mayadas-Shatzkes (MS) theory and temperature dependence incorporated in bulk conductivity, spatially-resolved FS (SRFS) and MS models. Based on this comprehensive modeling approach, we develop a 3D simulation framework for copper-based tapered via structure with Ta liner and TaN barrier to evaluate the via resistance. Our results show that the temperature-sensitivity of via resistance mainly stems from the bulk conductivity of copper. Utilizing our physics-based SRFS model, we confirm that the resistance due to surface scattering has a negligible temperature-dependence across a wide range of specularity and interconnect dimensions.

3:30 – 3:50 Coffee Break

Session 14: Materials & Unit Process III

Chair: Axel Preusse (Global Foundries)

3:50 – 4:10

14.1 Improvement of Ru-Co Liner for void-free Cu interconnect in extremely small pitch

hehsang Ahn, Seungwook Lee, Hoyun Jeon, Wonhyuk Hong, EunJi Jung, Taehong Ha – Samsung Electronics

While development in Copper (Cu) processes can contribute to Cu fill enhancement, optimizing the properties of the Liner can also be a significant role in Cu reflow characteristics. Therefore, this study aimed to improve Cu fill through the enhancement of the Ruthenium (Ru) and cobalt (Co) liner, particularly on 3nm-scale Cu interconnects. The surface morphology of the RuCo liner, which appears as the Co thickness increases, was improved through Atomic Layer Deposition (ALD)-like deposition of Co layer and plasma treatment between liner layers. This work provides the way to improve RuCo liner through process enhancements, resulting in a 80% reduction in void formation and enhancing Cu reflow characteristics. In addition, it was confirmed that the improved RuCo liner generates less voids depending on between chemical mechanical planarization (CMP) step to BM seed step.

4:10 – 4:30

14.2 Atomic Layer Deposition of TiN in Horizontal Vias Using Hydrazine as Nitrogen Precursor *(Student Paper)*

Jannick Fammels, Ping Che Lee, Dipayan Pal, Julian Pilz, Dmytro Solonenko, Jeffrey Spiegelman, Andrew Kummel – University of California, San Diego; Silicon Austria Labs, RASIRC

With decreasing feature size and changes in 3D DRAM and NAND architecture, TiN diffusion barriers for Cu and W metallization must become thinner and extremely conformal in horizontal structures. Titanium tetrachloride (TiCl4) and anhydrous hydrazine (N2H4) are promising precursors for low resistivity TiN atomic layer deposition (ALD). In this work these precursors were investigated for developing a particle free TiN ALD process with extremely high conformality in horizontal vias.

4:30 – 4:50

14.3 Ultra Low-k Properties of Atomic Layer Deposited Amorphous Boron Nitride for Futuristic Inter Metal Dielectric

Inkyu Sohn, Taejin Choi, Jaewon Kim, Hyungjun Kim – Yonsei University, Samsung Electronics

Here, we report 4 nm thick a-BN films deposited by plasma enhanced atomic layer deposition (PE-ALD) with ultralow k values of 1.43 (close to that of air, k = 1) at operation frequencies of 1 MHz. The growth per cycle (GPC) is confirmed to be ~0.12 A/cycle at 350 °C; and the thickness of synthesized film linearly increased with the number of ALD cycles. The RMS roughness is only 1.23 nm even at 30 nm thick of a-BN which indicates the formation of smooth surface of our ALD process. Also, XPS shows the stoichiometric a-BN and TEM, XRD, Raman confirms the amorphous nature of BN. Our results demonstrate that ALD a-BN process holds the potential for application in the realization of next-generation 3D integrated devices.