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2022 IITC Workshop and Conference Program

MONDAY, JUNE 27, 2022

Workshop

Perspectives on Heterogeneous Integration and Packaging for Advanced Technologies

CHAIR: Nick Lanzillo

9:00 – 10:00

When Chips Become Systems: An introduction to advanced 3D packaging for chiplet-based architecture

John Park – Cadence

In the spirit of More-than-Moore, design teams are turning to advanced packaging techniques involving multiple chiplets to meet today's demands of increased functional density, higher bandwidths and lower power products. Helping to accelerate this trend, the large IC foundries are now competing with the traditional packaging solution providers (OSATs) by providing their own back-end/packaging solutions based on wafer-level manufacturing techniques. The result is an explosion in the number of packaging technologies, pivoting the world of semiconductor packaging from a necessary evil to a value-add technology. From this presentation, you will learn about trends in advanced multi-chip(let) design, definitions to new terms like heterogenous integration, and challenges for package and IC designers when migrating to cutting-edge 2.5D and 3D packaging solutions.

10:00 – 11:00

Reliability Assessment for Heterogeneously Integrated Package

Ganesh Subbarayan – Purdue

Heterogeneous Integration provides a powerful and cost-effective means for building complex Systems-in-Package (SiPs). Recently, sophisticated examples of heterogeneously integrated packages containing nearly 50 dies, many fabricated by different vendors on different technological nodes, have been demonstrated. In general, integration of large number of dies leads to a polynomial increase in material interfaces, which are potential locations for increased thermal resistance and mechanical fracture. Also, the larger sized multi-die packages result in complex chip-package interactions, while the smaller solder bump size results in joints that are largely made of brittle intermetallic compounds. In this talk, I will broadly describe the reliability concerns in heterogeneously integrated packages and illustrate through examples the thermo-mechanical behavioral characterization necessary for their reliability assessment. Specifically, I will describe (1) an assessment of stress induced by Through Silicon Vias (TSV) and its impact on mobility (2) the reasons for package-caused fracture in back-end-of-line (BEOL) structures (referred as chip-package interaction) (3) the effect of thermal expansion mismatch between the mold compound and silicon on fracture in BEOL structures and (4) modeling and experimental characterization of phase growth under current and elevated temperature (electromigration) in

microbumps. Underlying the examples are sophisticated multiphysics computational models for moving (crack or phase) boundaries as well as fabricated test devices.

11:00 – 12:00

Dense, Scalable and Self-Aligning 2.5D and 3D IC Technologies

Muhannad Bakir – GIT

Monolithic ICs have progressed at an unprecedented rate of innovation in the past 60 years. But, due to performance, energy, and cost considerations, 2.5D and 3D 'polylithic ICs' have emerged as key enablers for the next phase of Moore's Law. This presentation will discuss various emerging polylithic integration approaches using 2.5D and 3D IC technologies, including those being developed at Georgia Tech's Integrated 3D Systems Lab. In particular, we first explore and benchmark scalable bridge-chip based 2.5D/3D IC technologies. Power delivery and thermal design considerations are also discussed and benchmarked for such technologies. Next, we discuss emerging 3D ICs technologies, including 3D Integrated Chiplet-Encapsulation (3D ICE), which enables the encapsulation of multiple chiplets using low-temperature SiO2 (ICP-PECVD) resulting in SiO2-reconstituted-tiers. Such reconstituted-tiers can then be stacked onto CMOS wafers to enable dense heterogeneous chiplet integration within BEOL. Lastly, we also discuss the possibility of using selective cobalt ALD deposition to form dense chip I/O bonds in 3D ICs. Unlike conventional bonding solutions, ALD-based chip bonding does not require any mechanical loads, is based on low-temperature processes, and has a higher-tolerance to surface imperfections in general.

12:00 – 13:30 Lunch

13:30 – 14:30

Computational Analyses Techniques for Signal Integrity of High-speed Interconnects and IC processing, Assembly and Reliability in 2D and 3DICs

Garth Sunberg & Dandan Lyu – ANSYS

Advanced simulation techniques and methodologies will be presented for the electromagnetic and signal integrity analyses of high-speed interconnects in 3DICs, silicon interposers and large chiplet-based SoCs. An EM-aware design flow will be discussed that aims to offer performance optimization of high-speed buses in the presence of power grid and package ground planes. A computational multiscale approach will be presented to link the information of mesoscale dissimilar solder ball geometries to the macroscale drop shock of a printed circuit board (PCB). A novel implicit incompressible smoothed particle Galerkin (ISPG) method is introduced to model the free-surface solder reflow process and predict the solder ball shapes. Subsequently, the predicted solder ball shapes from the reflow analysis are used in a chip package model for the drop shock analysis. The mesoscale solder joint model is coupled concurrently with the macroscale chip package model using an explicit-explicit non-intrusive two-scale coupling method via the co-simulation technique.

14:30 – 15:30

Multiphysics Design Automation and Optimization for Heterogeneous Integration

Dan Jiao – Purdue

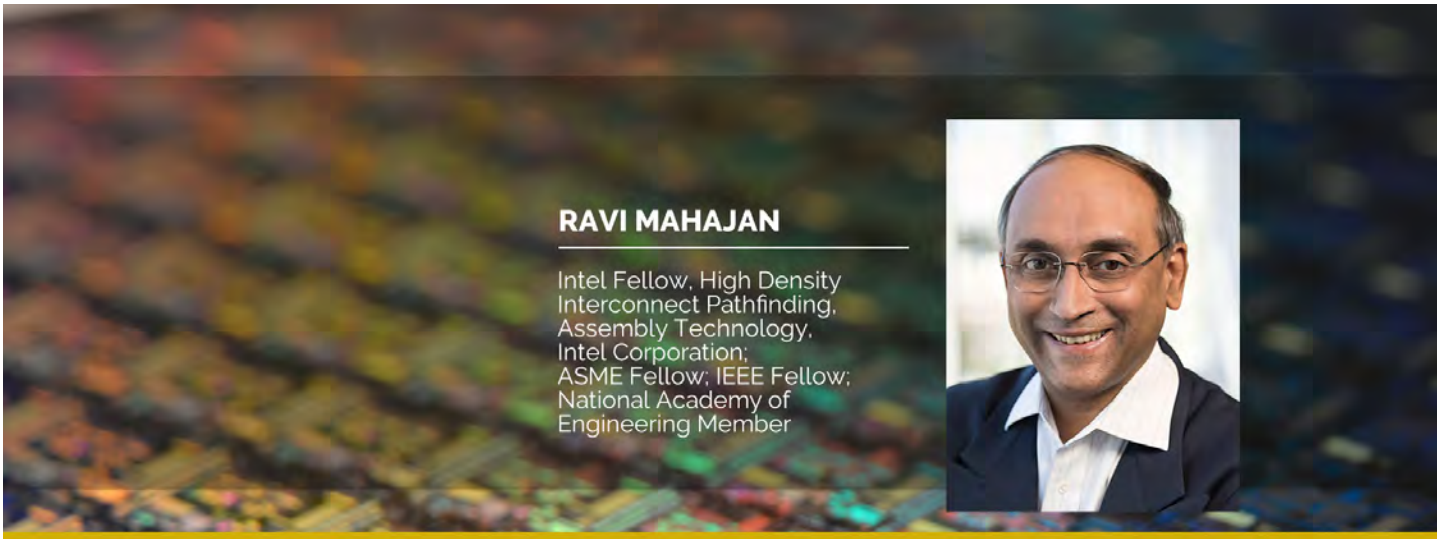
Heterogeneous Integration (HI) has shown tremendous potential to overcome the limitations and shortcomings of current monolithic integration technology, and effectively combat the slow-down of Moore's law. Currently, HI is impeded by the lack of tools seamlessly integrated for system-level design automation and optimization, and it has become a bottleneck of the design flow. Unlike the design automation and optimization of on-chip design, the package and system design for HI remains largely manual, tedious, time consuming, non-optimal, and error prone. The design time from intent to finish for a complex system is unacceptably large, yet only a small fraction of the design space is explored. The design automation and optimization of HI is challenging because it must (1) simultaneously address the electrical, electromagnetic, optical, thermal, mechanical, and reliability challenges of integrating separately designed and manufactured components into a high-level system, (2) account for a diverse range of applications ranging from high-performance computing to autonomous vehicles, and hence vastly disparate integration needs and system requirements. In this talk, I will review the needs, challenges, key building blocks, and recent advances in multiphysics-informed design automation and optimization of HI.

15:30 – 16:30

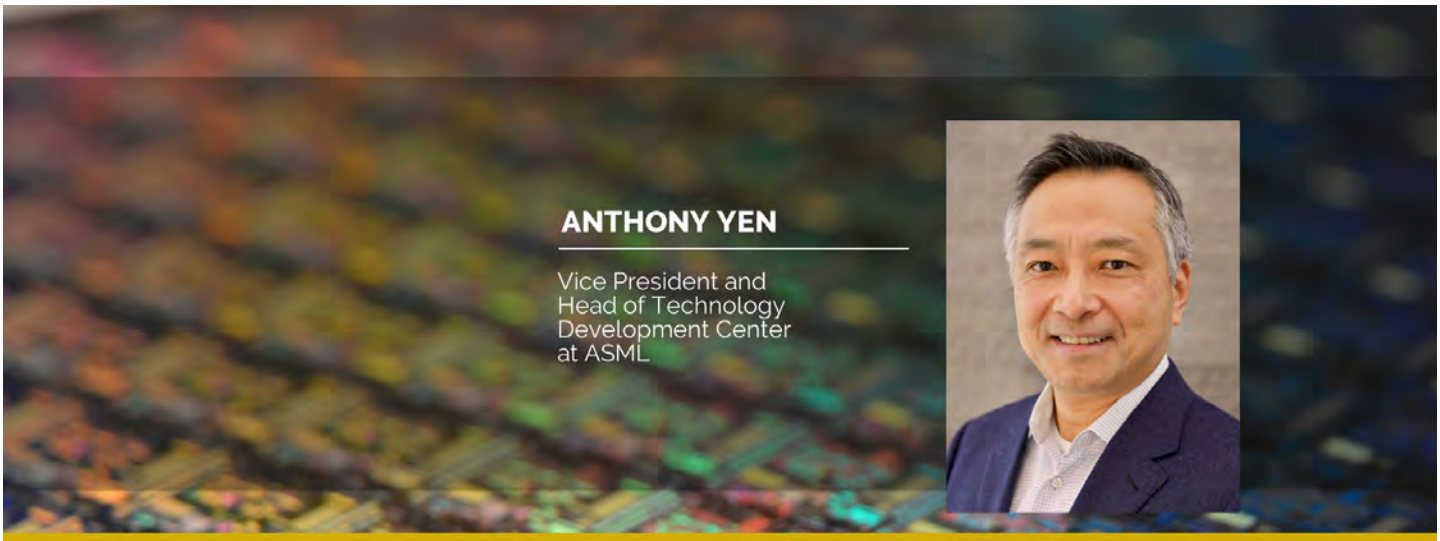
Peel and Stack: Ultimate Heterogeneous Integration for Next Generation Electronics$

Jeehwan Kim – MIT

For future of electronics such as bioelectronics, 3D integrated electronics, and bendable electronics, needs for flexibility and stackability of electronic products have substantially grown up. However, conventional wafer-based single-crystalline semiconductors cannot catch up with such trends because they are bound to the thick rigid wafers such that they are neither flexible nor stackable. Although polymer-based organic electronic materials are more compatible as they are mechanically complaint and less costly than inorganic counterparts, their electronic/photonic performance is substantially inferior to that of single-crystalline inorganic materials. For the past half a decade, my research group at MIT has focused on mitigating such performance-mechanical compliance dilemma by developing methods to obtain cheap, flexible, stackable, single-crystalline inorganic systems. In today's talk, I will discuss about our strategies to realize such a dream electronic system and how these strategies unlock new ways of manufacturing afvanced electronic systems. I will highlight our 2D materials-based layer transfer (2DLT) technique that can produce single-crystalline freestanding membranes from any compound materials with their excellent semiconducting performance. In addition, I will present unprecedented artificial heterostructures enabled by stacking of those freestanding 3D material membranes, e.g., world's smallest vertically-stacked full color micro-LEDs, world's best multiferroic devices, battery-less wireless e-skin, and reconfigurable hetero-integrated chips with AI accelerators.



KEYNOTE #1: **Directions, Challenges and Opportunities in Heterogeneous Integration**, Ravi Mahajan



KEYNOTE #2: **EUV Lithography: What's Up and What's Next** , Anthony Yen

TUESDAY, JUNE 28, 2022

Session 1: Conference Kick-off and Awards Program

8:15 – 8:25
Welcome
Hui Jae Yoo – AMAT

8:25 – 8:35
Award Program – Best Papers 2021

Keynote Talks

8:35 – 9:25
Keynote – Directions, Challenges and Opportunities in Heterogeneous Integration
Ravi Mahajan – Intel
Heterogeneous Integration is a powerful and crucial enabler for the continued growth of computing performance. Advanced packaging technologies are critical enablers of Heterogeneous Integration (HI) because of their importance as compact, power efficient platforms. This talk will focus on the tremendous opportunities in different application environments and focus on the projected evolution of advanced packaging architectures. Different advanced packaging architectures will be compared on the basis of their physical interconnect capabilities, power delivery, power removal, and high bandwidth signaling capabilities. Specific examples, showing how product implementations take advantage of these technologies, to provide an unprecedented level of performance, will be used to describe the challenges and opportunities in developing robust advanced package architectures. In addition to performance characteristics, this talk will also illustrate key opportunities and challenges in materials development, manufacturability, metrologies and reliability, and describe how well defined industry-academia partnerships can continue to ensure successful evolution of the HI roadmap.

9:25 – 10:15
Keynote – EUV lithography: what's up and what's next
Anthony Yen – ASML
Nanolithography enables today's intelligent society and extreme-ultraviolet (EUV) lithography is the latest enabling lithographic technology. ASML's EUV exposure systems are being used in the high-volume production of semiconductor logic and memory chips. In the words of Professor Jesús del Alamo of MIT, "It's an absolutely revolutionary product, a breakthrough that is going to give a new lease of life to the industry for years." For this presentation, I will start with a brief history of the development of EUV lithography and then present the technology's present status,

including its use in the manufacture of logic integrated circuits. Finally, I will give a progress report on our next-generation EUV exposure systems and an outlook of EUV lithography for the remainder of this decade.

10:15 – 10:35 Coffee Break

Session 2: 3D Integration and Advanced Packaging

CHAIR: Andrew Yeoh

10:35 – 11:05

2.1 Heterogeneous Integration for AI Architectures (Invited)

Mukta Farooq – IBM Research

Abstract

11:05 – 11:35

2.2 Ponte Vecchio : Building a Foundation to Enable 1000X Scaling for the Third Dimension of Moore's Law (Invited)

Wilfred Gomes – Intel Corporation

This talk covers the technology pipeline to get to Zetta Scale. We build on the foundation around our Data center GPU architecture, codenamed Ponte Vecchio (PVC). PVC enables a new class of Exaflop HPC/AI super computers implemented using active Logic on Logic 3D stacking with Foveros and EMIB and incorporates over 100B transistors spread across 47 tiles and 5 process nodes to deliver >1 Peta ops performance and enables exaflop computing. Using this as the background - we describe the challenges and directions in logic, memory, power delivery and IO needed to get to Zetta scale this decade.

11:35 – 12:00

2.3 Pixel Pitch Hybrid Bonding and Three Layer Stacking Technology for BSI Image Sensor

Kazumasa Tanida*, Shigeru Suzuki, Toshiki Seo, Yasunori Morinaga, Hayato Korogi, Michinari Tetani, Masakazu Hamada, Ryuji Eto, Takeshi Yamashita, Yasuhiro Kato, Naoaki Sato, Tadami Shimizu, Tetsuro Hanawa, Hiroko Kubo, Kenji Ueda, Fumitaka Ito, Yoshihiro Noguchi, Masayuki Nakamura, Ryuji Mizukoshi, Masahiko Takeuchi, Masakatsu Suzuki, Naoto Niisoe, Isao Miyanaga, Atsushi Ikeda, Susumu Matsumoto – Tower Partners Semiconductor

We have developed a pixel pitch (1.35 µm) hybrid wafer bonding technology and successfully demonstrated three layer stacked backside illuminated (BSI) image sensor fabrication with full hybrid Cu-Cu direct bonding process. We found that plasma activation condition on the bonding wafer surface is a key factor of Cu-Cu contact yield improvement for smaller size Cu contacts. Optimized pixel pitch hybrid bonding shows good electrical and reliability performances. For three layer stacking, we developed through Si via (TSV) process. The second hybrid bonding process was adapted on the first hybrid bonded wafers and it shows good electrical performances. This three layer stack technology with pixel pitch hybrid bonding is promising for many different applications.

12:00 – 13:20 Lunch

Session 3: 3D Integration and Advanced Packaging

CHAIR: Chris Wilson

13:20 – 13:50

3.1 Cu Hybrid Bonding Process Key Challenges and Solutions to C2W and W2W Bonding Applications (Invited)

Wei Zhou – Micron

Cu-Cu bonding is getting popular in industrials due to its excellent electrical and thermal performance. However extreme challenges are present in the assembly processes as compared with traditional solder based interconnection technologies. This talk will elaborate some of the key challenges we have experienced in the Cu pillar to Cu pillar bonding and Cu/dielectric hybrid bonding process development. In particular focuses will be on how to enable Cu hybrid bonding in the High Bandwidth Memory (HBM) packaging solutions in the forms of chip to wafer (C2W) and wafer to wafer (W2W) stackings. Areas investigated include Cu surface oxidation removal, plasma activation, Cu pad dishing control and most importantly how to minimize the particle's impact. Dielectric material, on the other hand, is a critical enabler too. The material selection needs to be compliant with the wafer carrier support system, which usually comprises of organic glue and its outgas must be eliminated in order to achieve a void-free surface to surface bonding. Innovations are compulsory to overcome all these challenges. Finally the discussions will involve the bonding strength characteristic method for a C2W stacking as the traditional Maszara test is no longer valid for an extreme thin die stacking.

13:50 – 14:20

3.2 Nanoengineered CTE Tailorable Copper Solder for Robust High Performance Heterogeneous Integration and Packaging (Invited)

Alfred Zinn – Kuprion Inc

Kuprion's engineered ActiveCopper is a highly conductive nanocopper-based, interconnect material that can be CTE adjusted over a wide range to solve our current packaging challenges electronics. The pressure-less sintering conditions are similar to solder (peak "reflow temperature around 220-240 C), with the sintered material exhibiting thermal and electrical conductivities close to that of bulk copper. Since the material converts to bulk copper upon fusion in a few minutes, its operating temperature can far exceed the original processing temperature. We have demonstrated high reliability in typical thermal shock environments of up to 4000 cycles in some cases for a wide variety of die attach form factors (1x1 mm to 25x25 mm). 3 x 3 mm dies bonded to patterned DBC AlN substrates for example show exceptional reliability in thermal shock and thermal cycling tests, with a 100% survival rate. Some parts survived multiple 100 kg shear loads after thermal shock without failing. Development of formulations for high density interconnects for SoC and SiP is in progress as well as materials for the economic large-scale filling of TSV and TGV.

14:20 – 14:45

3.3 TSV fabrication technology using direct electroplating of Cu on the electroless plated barrier metal

Shoso Shingubara*, Tomohiro Shimizu, Kosuke matsui, yuko miyake, Yuichiro Torinari, Makoto Motoyoshi, Shigeru Watariguchi, Hideki Watanabe – Kansai Univ

We propose a new TSV fabrication process using electroless plating of a barrier metal layer in TSV, and succeeding direct electroplating of Cu on the barrier without Cu seed layer. The conformal and thick (> 50 nm) CoWB barrier layer deposition inside a high aspect ratio TSV enables direct electro-plating of Cu from top to bottom of TSV entirely. Uniformity of CoWB thickness is within 10 % in 8 inch wafer. Furthermore, we successfully fabricated a daisy chain of TSV of 1200 steps and evaluated electrical properties. Excellent endurance property of the TSV daisy chain was obtained without any change of the resistance. This technology is promising for the 3-D LSIs that uses high aspect ratio TSVs.

14:45 – 15:05 pm Coffee Break

Session 4: Memory and Emerging Technologies

CHAIR: Philippe Rodriguez

15:05 – 15:35

4.1 A Materials to Systems Understanding of a BEOL Embedded Analog NVM Memory Technology for Edge Compute Applications (Invited)

Michael Chudzik – AMAT

Multi-Level Cell (MLC) ReRAM is essential for future analog Compute In-Memory (CIM) systems, where the weights of Neural Networks (NN) are stored in on-chip low-power devices. For large NN, tile-based architectures are used to map weights across multiple crossbar arrays, and low ReRAM conductance states are required to enable larger array size and reduce power consumption. Additionally, these ReRAM materials need to be compatible with modern BEOL architectures with the restricted thermal budgets and integration environments. MLC behavior has been demonstrated in filamentary ReRAM (f-ReRAM) but it suffers from abrupt, stochastic switching due to random movement of discrete defects in the conductive filaments. In this work, we introduce a new class of non-filamentary b-ReRAM bitcells featuring 128 programmable states. Ultra-low current is achieved thanks to our unique group-IV silicate multilayer stack, enabling a larger array size and increased compute density. The devices are fabricated with 65nm 1T1R structure in the BEOL using a custom 300mm deposition system with high wafer-level yield and uniformity.

15:35 – 16:05

4.2 Demonstration of HfO2-based BEOL-integrated ferroelectric memories: current status and future challenges (Invited)

Laurent Grenouillet – CEA-Leti

Ferroelectric hafnium oxide was unveiled only 11 years ago. Thanks to its CMOS compatibility and potential for scalability, this material not only changes the paradigm of ultra-low power ferroelectric random access memories (FeRAM), but also opens new perspectives for in-memory computing.

In this talk I will report on our recent work on ferroelectric hafnia, with a focus on 1T-1C FeRAM arrays for memory applications. After a description of HfO_2-based scaled

Metal/Ferroelectric/Metal capacitor integrated in the Back-End Of Line of 130nm CMOS, a performance overview will be given on 1T-1C FeRAM arrays which provide statistically relevant data. Finally, the main challenges and perspectives regarding the scalability of this technology will be discussed.

16:05 – 16:35

4.3 Via-switch FPGA with Transistor-free Programmability (Invited)

Masanori Hashimoto – Kyoto University

FPGA is providing a design platform suitable for AI applications being updated every day thanks to its field programmability. However, the field programmability is attained at the cost of a huge silicon area, which degrades FPGA performance. To overcome this issue, we have developed via-switch FPGA which uses via-switch crossbars in BEOL for programmability instead of transistors in FEOL. This talk highlights the freedom of computing architecture under the via-switch crossbars and shows the opportunity of near-memory massively-parallel computation.

16:35 – 17:00

4.4 Carbon Plug Application in 3D NAND Fabrication

Yu Chih Chang, Liang-Yu Chen, Kuang-Wei Chen*, Tuung Luoh, Ling-Wuu Yang, Ta-Hone Yang, Kuang-Chao Chen – Macronix International Co. Ltd.

The most efficient way to increase storage capacity is to add more layers stacked in 3D NAND device. Carbon plug fill and carbon CMP processes are implemented at the 1st tier deck channel holes to protect the damage from 2nd tier deck HAR etch drilling. Coventor SEMulator3D is adopted to speed up the process tuning of deposition/ etch/ deposition carbon plug fill-in. High selectivity carbon CMP process removes the overburden of carbon material then keep the flatness with good defect performance are the key module for multi-tiers decks in 3D NAND fabrication.

17:00 – 17:25

4.5 Low Temperature 90nm Pitch Invertigations for BEOL Quantum Applications

Roselyne Segaud, Patrice Gergaud, Stephane Minoret, Paul Neuman, Frederic Gustavo, Agnes Royer, Christophe Licitra, Denis Mariol, Fatrice Nemouchi – CEA-Leti

Superconducting BEOL might be crucial for quantum applications. In the present work, detailed studies of Ta and TaN behavior are reported. While bulk Ta and TaN are superconducting, the TC is affected by deposition conditions and layer thickness. However, 9 nm of Ta deposited on TaN leads to reach a TC of 2 K. The second part of this paper reports a huge intrinsic thermal expansion coefficient (TEC) whatever the ULK porosity. The huge TEC can drive to strong residual stress that could affected the superconductivity of the metal line.

WEDNESDAY, JUNE 29, 2022

Session 5: Reliability

CHAIR: Mark Zaleski

8:15 – 8:40

5.1 Effects of composition deviation of CuAl2 on Electromigration

Toshihiro Kuge*, Masataka Yahagi, Junichi Koike – Tohoku Univ

This paper reports the effect of composition deviation of CuAl2 on electromigration (EM) property. EM property was measured in the temperature range of 225-325 °C at a current density of 1 MA/cm2. At 275 °C, the void formation rate of Al-rich sample was found to be 1.1-1.2 times faster than that of stoichiometric samples, while it was reduced to 1/5 for Cu-rich samples. The activation energy of Al-rich and stoichiometric samples is found to be 1.16 eV, while that of Cu-rich sample is 1.59 eV. These results show that shifting the composition to Cu-rich side enhances the electromigration properties and the composition has been found to have a significant effect on electromigration of intermetallic compounds.

8:40 – 9:05

5.2 Dynamics of electromigration voids in Cu interconnects: investigation using a physics-based model augmented by neural networks

Ahmed S. Saleh*, Houman Zahedmanesh, Hajdin Ceric, Kristof Croes, Ingrid De Wolf – IMEC

Physics-based numerical simulations have been widely employed for understanding electromigration (EM) induced voiding in Cu interconnects. Yet, their application has remained limited to exploratory studies given their computational cost. To achieve fast, yet accurate, void dynamics simulations, in this study, a neural network (NN) is trained to determine local current density distributions around void surfaces. Up to 85% reduction of computational time was achieved by replacing the finite- element (FE) solver with the NN. The model was used to investigate the impact of interconnect linewidth, line and via aspect ratio and microstructure on void dynamics.

9:05 – 9:30

5.3 Reliability Evaluation of Semi-damascene Ru/Air-Gap interconnect with Metal Pitch down to 18 nm

Alicja Lesniewska*, Olalla Varela Pedreira, Philippe Roussel, Giulio Marti, Ankit Pokhrel, Marleen H. van der Veen, Stefan Decoster, Martin O'Toole, Gayle Murdoch, Ivan Ciofi, Seongho Park, Zsolt Tokei, Kristof Croes – IMEC

We evaluated the reliability of Semi-Damascene interconnects system fabricated by direct metal etch of Ru and Air-Gap as inter-metal dielectric. We show that intrinsically Ru does not drift into SiN and SiCO. Line-line TDDB results with Air-Gap widths of 8-16 nm (fixed line width of 10 nm) show a higher field acceleration factor compared to Dual-Damascene Ru/low-k systems and pass 10 years lifetime with Vmax > 0.75 V at 100oC for industry relevant line lengths. To address concerns related to moisture intake in Air-Gaps, we carried out humidity tests which showed no

significant change in capacitance, leakage and VBD after 1000h at 85C/85%RH. We also present that fully self-aligned vias pass electromigration and thermal storage tests.

9:30 – 9:55

5.4 Reliability benchmark of various via prefill metals

Olalla Varela Pedreira*, Veerle Simons, Marleen H. van der Veen, Ivan Ciofi, Seongho Park, Zsolt Tokei, Kristof Croes, Shirish Pethe, Wei Lei, Shinjae Hwang, Zhiyuan Wu, Feng Chen, Alexander Jansen, Jerome Machillot, Andrew Cockburn – IMEC

We show that filling vias with refractory metals deposited barrierless (like W or Ru) eliminate the reliability concerns raised in previous studies on Co via prefill. In particular, we characterized the reliability of W-Cu hybrid systems landing on Ru and Co and compare them with earlier results using Co and Ru via prefill. Via electromigration results show expected parameters for systems with SiCN cap and failure analysis after via electromigration shows no voiding in the W vias. Long term thermal storage experiments for 1200 h indicate that W vias are reliable and do not suffer from voiding or metal intermixing.

9:55 – 10:20

5.5 Failure Mode Analysis in Microsecond UV Laser Annealing of Cu Thin Films

Remi Demoulin, Richard Daubriac, Louis Thuries, Emmanuel Scheid, Fabien Rozé, Fuccio Cristiano, Toshiyuki Tabata, Fulvio Mazzamuto – LAAS-CNRS

The need of surface-localized thermal processing is strongly increasing especially w.r.t three-dimensionally (3D) integrated electrical devices. UV laser annealing (UV-LA) technology well addresses this challenge. Particularly UV-LA can reduce resistivity by enlarging metallic grains in lines or thin films, irradiating only the interconnects for short timescales. However, the risk of failure in electrical performance must be correctly managed, and that of UV-LA has not been deeply studied yet. In this work microsecond-scale UV-LA is applied on a stack comparable to an interconnect structure (dielectric/Cu/Ta/SiO2/Si) in either melt or sub-melt regime for grain growth. The failure modes such as (i) Cu diffusion into SiO2, (ii) O incorporation into Cu, and (iii) intermixing between Cu and Ta are investigated.

10:20 – 10:40 AM Coffee Break

Session 6: Unit Process and Integration

CHAIR: Nick Lanzillo

10:40 – 11:10

6.1 Recent Progress in Graphene Processes for Metallization and RF Applications (Invited)

Kazuyoshi Ueno – Shibaura Institute of Technology

Research on graphene processes for the applications to interconnects and electrodes, such as graphene caps, direct deposition of multi-layer graphene, and stable intercalation doping, is steadily progressing. Furthermore, attention will be paid to the application of graphene, which has a high kinetic inductance, to RF devices. Here, I will give an overview of recent research trends toward the practical application of graphene and discuss the issues.

11:10 – 11:40

6.2 Advanced process technologies for continuous logic scaling towards 2nm node and beyond (Invited)

Tomonari Yamamoto – Tokyo Electron Limited

This invited talk describes the advanced process technologies for continuous logic transistor and interconnect evolution towards 2nm node and beyond. Gate-all-around (GAA) improves electrostatics over FinFET and enables continuous gate length scaling. Complementary FET (CFET), which is a structure of stacked transistors, is a next candidate architecture for the continuous cell height scaling enablement. Interconnect pitch scaling will also play crucial role for it and go with RC reduction knobs such as Cu extension, Post Cu and airgap. For better area usage and performance enhancement, backside power delivery network (PDN) is an attractive option. For these enablement, continuous process and tool advancement is necessary not only on film, etch, lithography and wet, but also on wafer bonding and thinning technologies. We will also review our recent progress in EUV related solutions including self-aligned patterning.

11:40 – 12:05

6.3 Computational Analysis of the Role of Nanoconfinement on the Reliability of ULK Glasses

Karsu Kilic, Reinhold Dauskardt – Stanford

ULK glasses exhibit significant changes in both their structure and properties under nanoscale confinement which they are exposed in microelectronic applications where ULK glasses such as hybrid organic-inorganic organosilicates (OSG) are deposited into nano-scale patterns in silicon wafers to perform as electrical insulators. It is crucial to elucidate the role of nanoscale device effects on different OSG materials and explore design strategies to limit extra degradation in mechanical properties. Accordingly, we present computational results showing that hyperconnected hybrid OSG precursors with cyclic organic rings assemble relatively more homogenously under confinement which leads to the formation of smaller scale nanovoids with superior mechanical reliability compared to more commonly used ethylene bridged OSG hybrids.

12:05 – 13:25 Lunch

Session 7: Unit Process and Integration

CHAIR: John Zhu

13:25 – 13:50

7.1 Improvement of Line-to-line TDDB by Cu and Barrier-metal Recess Structure for high voltage circuit in 3D Flash Memory

Mitsuhiko Noda, Kotaro Fujii, Naomi Yanai, Tsubasa Watanabe, Atsushi Kato, Kosuke Horibe, Eiru Yoshida, Tatsuhiko Koide, Hiroshi Fujita, Yumi Nakajima, Masayoshi Tagami, Kazuya Ohuchi – Kioxia Corporation

Cu interconnect structure is investigated to improve TDDB property of Cu line-to-line with scaled pitch in high voltage circuit for 3D flash memory. Recessed Cu and barrier-metal structure reduce unexpected local electric field concentration, and suppress Cu2+ or other cations drift into intra metal dielectrics. Those result in better reliability characteristics regarding TDDB life time than that of conventional structure.

13:50 – 14:15

7.2 Enabling 3-level High Aspect Ratio Supervias for 3nm nodes and below

Daniel Montero, Victor Vega Gonzalez, Yannick Feurprier, Olalla Varela Pedreira, Noriaki Oikawa, GERARDO Martinez, Dmitry Batuk, Harinarayanan Puliyalil, Janko Versluijs, Hanne De Coster, Nina Bazzazian, Nicolas Jourdan, Kaushik Kumar, Frederic Lazzarino, Gayle Murdoch, Seongho Park, Zsolt Tokei – IMEC

High aspect-ratio (AR) 3-level Supervias (SV), with a minimum bottom CD of 15.5 nm and AR = 7.7 are successfully integrated in a 3nm node chip. 3-level SV directly connects Mx with Mx+3 metal layers, without connecting to the intermediate two metal layers. Enabling such high AR SV is achieved by fine tuning the SV etch process to guarantee uniform SV landing and a straight vertical profile. Electrical results show that 3-level Kelvin SVs provide an average resistance of 58Ω, yielding > 95 % for the best conditions, improving our previously reported yield values of 2-level with enhanced AR [1]. 3-level SVs gave a resistance 13% lower than the conventional 2-level stacked via configuration [2]. Metallization stack used was 0.3 nm of ALD TiOx as an adhesion layer, followed by a Ru CVD deposition of 70 nm. Thermal shock tests of 500 hours, between -50°C and 125°C, performed on intervals of 15 min each, showed that the Kelvin resistance values remained virtually unchanged. Therefore, 3-level SV are stable after thermal shock tests, proving that they are a robust scaling booster for the 3nm node.

14:15 – 14:40

7.3 Galvanic Corrosion Effect of Co Liner on ALD TaN Barrier

Junki Jang, Changhyun Kim, Youngsoo Yoon, Yun Ki Choi, Hoon Kim, Jungil Park, Jaehyeong Park, Minguk Kang, Youngwoo Kim, Seonguk Jang, Junghwan Ahn, Eunyoung Park, Wonmin Jeong, Jeongjae Kim, Minhyuk Oh, Wonkyu Han, Dongwoo Shin, Wookhwan Kim, Jaeyoung Yang, Honglae Park, Segab Kwon, Jeong Hoon Ahn, Dr. Ku, Jahum – Samsung Electronics

This paper describes strong galvanic corrosion effect of Co liner on atomic layer deposition (ALD) TaN barrier during Cu CMP. Compared to Co liner on physical vapor deposition (PVD) TaN, Co liner on ALD TaN was more easily corroded resulting in Cu void defects. We investigated characteristic differences between ALD and PVD TaN, and identified the root cause of Cu void formation is higher nitrogen content in ALD TaN film. We could minimize the galvanic corrosion and the resulting Cu voids by reinforcing plasma treatments after ALD TaN deposition.

14:40 – 15:00 PM Coffee Break

Session 8: Advanced Interconnects

CHAIR: Paul Besser, Kisik Choi

15:00 – 15:30

8.1 Advanced interconnect technology for 2nm node and beyond (Invited)

Jinnam Kim – Samsung Electronics

The device nodes of 2nm and beyond face great challenges on performance, power, area and cost since the patterning needs more EUV layers and the resistance of contacts and wires increase as the interconnect scales down. Industries are struggling to extend Cu interconnect by reducing

barrier metal thickness and implementing selective barrier metal, however, the resistance is already higher than the values required to meet the device performance target. Alternative metals can be the solution of these challenges due to its low resistivity at the line width smaller than around 10 nm. Also, it gives chances to grow the single grain at the hole type patterns and deposit metals selectively from the via bottoms. Furthermore, direct metal etch scheme can be considered with alternative metals, which provides the lower resistance than damascene at same aspect ratio and the easy way to make airgap between patterned wires. Direct etch schemes with airgap can be the only solution to achieve the low resistance and the low capacitance at the same time. Another disruptive solution is to adopt new schemes such as backside power delivery network and buried power rail, which enable more wide wires for delivering power on the backside of the wafer and give more spaces to route in the interconnect layers at the front side of the wafer. However, it entails difficult techniques of wafer bonding, thinning, and making nano-sized TSV. Also we have to choose proper metallization to fill the TSV to have low resistance with less defects.

15:30 – 15:55

8.2 Metal-Induced Line Width Variability Challenge and Mitigation Strategy in Advanced Post-Cu Interconnects

Koichi Motoyama, Nick Lanzillo, Sagarika Mukesh, Cornelius Brown Peethala, Terry Spooner, daniel edelstein, Kisik Choi – IBM

This study illustrates that the mechanism of line wiggling (repetitive line CD variability) caused by post-Cu alternative metals deposition can be characterized by a “zipping up” behavior of alternative metals, which is related to their surface energy. The repetitive line CD variability caused a line resistance increase, which resulted in overall circuit performance degradation. It has been observed that the extent of line wiggling has strong dependencies on several parameters such as A/R (Aspect Ratio) of trenches and the modulus of IMD (Inter Metal Dielectric). We have demonstrated Ru interconnects without line wiggling by using a sacrificial TiN template which is replaced with low-k material after line fabrication.

15:55 – 16:20

8.3 Barrierless ALD Molybdenum for Buried Power Rail and Via-to-Buried Power Rail metallization

Anshul Gupta, Jan Willem Maes, Nicolas Jourdan, Chiyu Zhu, Sukanya Datta, Olalla Varela Pedreira, Quoc Toan Le, Dunja Radisic, nancy heylen, Antoine Pacco, Shouhua Wang, Moataz Mousa, Young Byun, Felix Seidel, Bart de Wachter, Gayle Murdoch, Zsolt Tokei, Eugenio Dentoni Litta, Naoto Horiguchi – IMEC

This work reports for the first time, a middle-of-line (MOL) compatible, barrier/liner-less ALD molybdenum (Mo) process on SiO2 used for Via-to-buried-power-rail (VBPR) and contact-to-active (M0A) dual damascene metallization. We also compare the MOL-compatible ALD process with the front-end-of-line (FEOL)-compatible ALD process used for BPR fill as reported in [1]. In addition, we report that Mo-BPR can withstand 800 °C anneal, demonstrating its compatibility with high thermal budgets of FEOL. Furthermore, we demonstrate for the first time, integrated (i.e. w/o air-break) precleans prior to Mo-VBPR deposition for contact formation with Mo-BPR. The precleans remove MoOx from Mo-BPR surface proven by SIMS characterization at blanket

film level. The effectiveness of precleans is further proven at via level with a good agreement between measured and predicted Mo-VBPR resistance (R) landing on Mo-BPR. Finally, the first downstream electromigration tests on Mo-BPR annealed at 800 °C show no failures for >150 h at 5 MA/cm2 & 330 °C proving its robust behavior.

16:20 – 16:45

8.4 MP18-26 Ru Direct-Etch Integration Development with Leakage Improvement and Increased Aspect Ratio

Ankit Pokhrel, Giulio Marti, Martin O'Toole, Gayle Murdoch, Anshul Gupta, Stefan Decoster, Souvik Kundu, Elisabeth Camerotto, Quoc Toan Le, Arame Thiam, Alicja Lesniewska, Seongho Park, Zsolt Tokei – IMEC

Ru semi-damascene has been recently considered as a promising candidate to replace the conventional Cu dual damascene to meet the continued RC scaling needs in sub-2nm technology nodes. In this work, Ru lines with critical dimension of 9-10 nm and AR 3-6 targeting MP18-MP26 were fabricated in IMEC 300-mm pilot line using EUV-SADP technique and subsequent direct etch of Ru films for the first time. We demonstrate the optimizations made in patterning, metal etch, and clean that enabled the successful fabrication of Ru lines. Single line resistance of 10µm Ru with AR 3 shows that >90% of the devices meet the resistance target of <700 Ω/µm for MP20-26 and ~50% for MP18. Leakage current measurements between the core-defined and gap-defined Ru lines show >90% of devices meet the leakage target of 10-11A/um.

16:45 – 17:10

8.5 Balancing Interconnect Resistance and Capacitance at the Advanced Technology Nodes based on Full Chip Analysis

Da Eun Shim, Azad Naeemi – GIT

This paper presents a technology-circuit co-optimization flow to achieve the best balance between wire resistance and capacitance in advanced technology nodes. It is shown that increasing the wire width to spacing ratio improves the circuit performance by up to 17.7%. In addition, we perform a sensitivity analysis on the resistance of interconnects within standard cells at the 7nm node where we show that a 2X hypothetical increase results in a 5.1% degradation in overall circuit performance, whereas a 0.5X hypothetical resistance improvement results in a 2.1% decrease in power.

Poster Session and Conference Reception (17:30 – 19:30)

Posters

CHAIR: Tatsuya Usami

P1. A new methodology for modeling Air-Gap TDDB

Yu Fang, Ivan Ciofi, Philippe Roussel, Alicja Lesniewska, Robin Degraeve, Davide Tierno, Ingrid De Wolf, Kristof Croes – IMEC

We present a methodology for predicting line-to-line reliability of Air-Gap schemes, which accounts for line edge roughness and electric field enhancement. Our model is calibrated to the intrinsic reliability properties of the Air-Gap interface dielectrics, which are characterized by performing time-dependent dielectric breakdown measurements on planar capacitors. We validate our model to experimental TDDB data from Ru/Air-Gap semi-damascene interconnects and predict that deeper Air-Gaps, extending into the bottom interlayer dielectric, can significantly boost the reliability of Air-Gaps schemes.

P2. Stress and thermal stress evolution in Mo and Ru thin films

Valeria Founta, Jean-Philippe Soulie, Shibesh Dutta, Ingrid De Wolf, Joris Van de Vondel, Johan Swerts, Zsolt Tokei, Christophe Adelmann – IMEC

In this work, the microstructural and stress evolution of Mo and Ru films is studied at relevant temperatures for interconnect processing. Wafer bow measurements, transmission electron microscopy (TEM), in-situ XRD (IS-XRD), and microelectromechanical systems (MEMS) were used to determine stress and thermal stress evolution for 10 to 30 nm thick films. We show that Mo and Ru present a complex evolution of the stress evolution during thermal cycling that can be linked to the creation and diffusion of point defects.

P3. Improved Resistivity of NiAl Thin Films at Low Temperature for Advanced Interconnect Metallization

Jean-Philippe Soulie, Zsolt Tokei, Johan Swerts, Christophe Adelmann – IMEC

We investigate NiAl as a potential alternative for Cu in future interconnect metallization schemes. NiAl was deposited by physical vapor deposition at temperatures up to 420ºC. A resistivity of 30 μΩcm was achieved for a 7 nm thick NiAl film at a deposition temperature of 420ºC with in-situ Si capping at 100ºC. A resistivity of 18 μΩcm was reached for 22 nm thick NiAl in identical conditions. Depositing epitaxial NiAl on Ge (100) led to an even lower resistivity of 14.3 μΩcm for a 22 nm film since better crystallinity was obtained. Challenges and integration feasibility are discussed. Keywords: Aluminides; alternative metals; thin films; resistivity; interconnect

P4. Low Resistivity Titanium Nitride Thin Film Fabricated by Atomic Layer Deposition with TiCl4 and Metal-Organic Precursors in Horizontal Vias

Cheng hsuan Kuo – UCSD

Titanium nitride (TiN) thin films are utilized as diffusion barriers for Co and W metal layers as well as the gate metal barrier in CMOS and memory devices due to the material's low resistivity; TiN is also used as a coating for hard disk drives[1]. Low resistivity TiN in commercial devices has been

deposited by plasma-enhanced ALD (PE-ALD) and by physical vapor deposition. However, for high aspect ratio features and horizontal vias, deposition by thermal ALD is needed to enhance the conformality of the deposition process. In the present work, it is shown that the resistivity can be decreased below 220 uΩ-cm with a non-halogenated precursor at 425 oC by using a Ti precursor with high thermal stability and by reducing the oxygen and carbon contents in the films using a highly reactive co-reactant, anhydrous hydrazine (N2H4). Titanium tetrachloride (TiCl4), as well as three metal-organic precursors and anhydrous hydrazine (N2H4, Rasirc, Brute Hydrazine), were employed with ultra-high purity nitrogen purge gas. Films formed with the three halogen-free precursors, TDMAT (tetrakis(dimethylamino)titanium), TDEAT (tetrakis(diethylamino)titanium), and TEMATi (tetrakis(ethylmethylamido)titanium) were compared to TiCl4 for resistivity and conformality. The TiN ALD chamber was connected to an in-situ Auger electron spectrometer (RBD Instruments), which determined the atomic composition of ALD TiN. Pulse lengths and purge times were optimized on HF-cleaned Si (100) or degreased SiO2. For TiCl4, the optimized deposition temperature was 425 oC and the optimal pulse times were 300 ms for TiCl4 and 3600 ms for N2H4, but for the metal-organic precursors, different optimized pulsed lengths and deposition temperatures were needed. Four-point probe (Ossila) measurements were performed to determine the resistivity of TiN thin films on degreased SiO2 substrates. Nanoscale patterned samples with horizontal vias (aspect ratio: 1:5) were used to verify the conformality of the low resistivity TiN thin films. TEM was employed to analyze the conformality of TiN thin films.

P5. Integration of Al2O3 Etch Stop Layer in 21nm Pitch Dual-Damascene BEOL interconnects

Chen Wu, Victor Vega Gonzalez, Hanne De Coster, Quoc Toan Le, Filip Schleicher, Alicja Lesniewska, Gayle Murdoch, Seongho Park, Zsolt Tokei – IMEC

To overcome the micro loading effect that happens during M2 trench etch, an Al2O3 etch stop layer is successfully implemented in our test vehicle with minimum 21nm metal pitch dual-damascene interconnects. Two integration challenges are investigated: via opening difficulty with 2nm Al2O3 layer and undercut issue with 5nm Al2O3 layer. Potential solutions are proposed accordingly. Post Ru metallization, good morphological and electrical results are demonstrated for the split with 5nm Al2O3.

P6. Developing a Low-Temperature Flip-Chip Bonding Technology with In/Au Microbumps to Suppress the Thermal Load on Spintronics Devices

Hisashi Kino, Takafumi Fukushima, Tetsu Tanaka – Tohoku Univ.

Spin transfer torque magnetic random-access memory (STT-MRAM) with magnetic tunnel junction (MTJ) devices, which are among the spintronics devices, have many advantages, such as high programing speed and sufficient endurance. Therefore, currently, the spintronics devices are being thoroughly studied. However, they suffer from low thermal stability; thus, low-temperature integration and packaging technologies need to be developed. In this study, we applied In/Au microbumps, which have low bonding temperature and high thermal stability, to a flip-chip bonded STT-MRAM onto a Si interposer. No effect of the flip-chip bonding process on the STT-MRAM cell was observed. Investigation results indicated that low-temperature bonding technology with In/Au microbumps are promising for accelerating the integration of spintronics devices.

P7. Effect of Current on Ni Catalyst Layer Used for Current-Enhanced CVD of Multilayer Graphene

Jumpei Tokida, Reno Hasumi, Kazuyoshi Ueno – Shibaura Institute of Technology

Current application was found to enhance the crystallinity of multilayer graphene during CVD using a Ni catalyst layer. However, the reduction of surface roughness has been the issue. The effect of current to the Ni catalyst layer was investigated, and it was found that the current promotes the growth of Ni (111) grains, leading to the enhanced compressive stress. After reaching the stress limit, the Ni microstructure changed again and the stress was relaxed. Such microstructure changes in the Ni film correlated with the surface roughness.

P8. Selective and Tunable Slurry for Advanced Packaging Epoxy Mold Compound

Shogo Arata, Chiaki Noda, Yasuhiro Ichige, Satoyuki Nomura, Trianggono Widodo, Nagatoshi Tsunoda, Xavier Brun – Showa Denko Materials Co., Ltd and Intel Corporation

Chemical mechanical polishing (CMP) process have been heavily utilized in throughout the semiconductor manufacturing processes from front-end to back-end for decades. However, CMP process is still in its early stage for advanced packaging because of the difficulties observed with implementation of CMP process such as: low removal rate, poor selectivity, and elevated surface roughness and defects on the organic polymer film. Nevertheless, CMP process is becoming an essential part of the 2D advanced packaging and beyond in order to achieve smaller pitch and improve re-distribution layer (RDL) process. In this paper, we focus on highly tunable removal rate and selectivity, and low defectivity performance slurry for epoxy mold compound (EMC) with silica filler and Cu pads.

P9. Schottky barrier height reduction by oxide layer insertion in Al/n-GaN structure

Jiro Koba, Masataka Yahagi, Junichi Koike – Tohoku Univ.

The purpose of this work is to obtain the low specific contact resistivity on n-GaN. We investigated the Schottky barrier height between various metals and GaN and found that Fermi level pinning occurred at the interface between metals and GaN. We also attempted to reduce the specific contact resistivity using MIS structure in order to release Fermi level pinning. We selected GaOx and TiOx for the insulator materials and obtained the low specific contact resistivity of 7.1×10^{-7} Ω·cm2 with GaOx on n-GaN having Si doping concentration of 2x1018 cm^{-3}

P10. A Novel Air-gap Formation Method for Metal Interconnect

Youngjoon Choi, Seong-Sik Jo – Philoptics

Electrospinning technology was introduced to the formation of air-gap in metal interconnection. A polyimide fiber-cluster layer was made with this technology on the line and space (L/S) patterns. After the hot melting of the layer, a perfect air-gap structure was created. It is different from the non-conformal CVD, and the sacrificial layer method. A polyimide nano-fiber-cluster layer (PI-nFCL) formed by E/S is changed into a dense polyimide (PI) film. Then it looks like a bridge on the patterns showing a perfect air-gap-like space.

P11. Wet processes deposition for HAR TSV metallization using electroless Co liner and alkaline Cu seed layer

Qu Xin-ping – Fudan Univ.
Through silicon via (TSV) with a high aspect ratio is in great demand in three-dimension (3D) integration technology. This work demonstrates a wet process flow for high aspect ratio TSV metallization using electroless cobalt deposition and copper electroplating. The electroless deposited Co liner and alkaline electroplating deposited Cu seed layer are successfully integrated into a 4 μm×50 μm TSV with an aspect ratio higher than 10:1. The electroless Co liner layer with a step coverage of up to 98% is formed on the TiN barrier by adding a suppressor additive in the plating bath. Then, a conformal alkaline Cu seed layer with step coverage of 75% is deposited on the Co liner layer throughout the TSV. Finally, the TSV is filled by the acidic Cu electroplating without voids, indicating the high quality of the Co liner layer as well as the Cu seed layer and the feasibility of the demonstrated wet process flow in the high aspect ratio TSV.

P12. Ru electrodeposition and behaviors of additives for advanced technology nodes
Youjung Kim, Haneul Han, Jinhyun Lee, Bongyoung Yoo – Hanyang Univ.
Ru deposition is required for advanced technology nodes (< 32 nm) because it can improve the performance with low resistivity in nanoscale features. This study reports electrochemical reactions of Ru and behaviors of additives on Ru electrodeposition using cyclic voltammetry (CV) and linear sweep voltammetry (LSV). Ru3+ forms complexes, and the complexes are reduced on the Ru surface. It was confirmed that disodium 3,3'-Dithiobis(1-propanesulfonate) (SPS) could accelerate Ru deposition, and polyvinylpyrrolidone (PVP) could suppress Ru deposition. Also, NaBr showed suppression, and it can form a strong suppression layer with PVP. Focused ion beam (FIB) image shows the filling of Ru with those additives.

P13. Electromigration Degradation of Gold Interconnects: A Statistical Study
Hajdin Ceric, Roberto Lacerda de Orio, Siegfried Selberherr – TU Wien
Electromigration induced degradation of gold metallization used for GaAs devices is a significant, but not sufficiently investigated phenomenon. In this work, a complete physics-based analysis of electromigration in gold is presented. In particular, the dependence of statistical failure features on the variation of geometric properties is investigated. The experimentally observed impact of the interconnect geometry on the mean failure time and the associated standard deviation of the failure times is well reproduced by numerical simulations.

P14. Scaling Down Diffusion Barriers: Performance and Thickness Dependence of TaN and Two-Dimensional-Material-Based Barrier Layers
Hippolyte Pierre Andre Georges Astier, Muhammed Juvaid Mangattuchali, Soumyadeep Sinha, Jing Yang Chung, Saurabh Srivastava, Chandan Das, John Sudijono, Silvija Gradecak – National Univ. of Singapore
Two-dimensional (2D) materials have been suggested to offer a viable route towards further miniaturization of interconnect technology as new diffusion barriers (DBs), replacing current industry standards at low thickness regime. We investigate new copper DBs to be used in back end of line (BEOL) interconnect structures, based on 2D materials grown on a large scale. The films are characterized using transmission electron microscopy, X-ray photoelectron spectroscopy and Raman spectroscopy to verify their structural quality and chemical composition. An experimental protocol is presented to assess the performance of these films as DBs, including

a device fabrication scheme and a measurement scheme that both allow for the comparison of different barriers. This study establishes the difference in barrier properties as a function of film thickness based on their different crystal structure, comparing 2D materials with industry standard TaN barriers, thus evaluating the potential of 2D materials for future, scaled down, interconnect technology. This screening protocol also enables optimization of the growth conditions for improved DBs.

P15. Change in resistivity of fine metal line by KrF excimer laser annealing

Yasutsugu Usami, Kaname Imokawa, Ryoichi Nohdomi, Kouji Kakizaki, Hakaru Mizoguchi – Gigaphoton Inc.

Regarding the resistance reduction in the fine metal line of the semiconductor device, the annealing effect by the excimer laser has been confirmed. KrF excimer laser irradiated to Cu and Ru as fine metal line materials, and the change in resistivity and the surface condition (change in the metal grain size) were confirmed. As a result, in Cu, the grain size doubled, and the resistivity decreased by about 20%. In Ru, the grain size expanded by about 1.2 times, and the resistivity decreased by about 10%. This experimental evaluation was performed by a KrF excimer laser with a pulse width of 82 ns and was found to have the lowest resistance just before the irradiation damage threshold (melting or ablation initiation value) in both cases.

P16. Cu to Cu direct bonding with optimized self-annealing behavior of the electroplated copper

Haneul Han, Chaerin Lee, Sangwoo Park, Youjung Kim, Bongyoung Yoo – Hanyang Univ.

Cu to Cu direct bonding at low temperature has required the driving force of the Cu films to self-diffuse each other. In this study, high defect density Cu was optimized with a mechanical property of the self-annealing phenomena. Furthermore, the mechanism of the defect generation was studied with electrochemical analysis. Based on the analytical study, Cu to Cu bonding with the high defect density Cu, which had high tensile strength, was successfully conducted at 250C bonding temperature.

P17. Conformal Copper ECD Metallization Process for deep TSV

Thomas Weidner, Volker Goetz, Theresa Roesch, Asmaa Bouhlal, Nik Wunder, Stephan Reinert, Kerst Griesbach, Manuela Goebelt, Hannes Mehner – X-FAB

This study highlights different aspects and challenges of through silicon via (TSV) metallization in a via-last approach in thick Wafers. The TSV-last process enables a modular TSV integration in already existing technologies without major design or process changes. The study focuses on the challenges of the metallization process of the TSVs, including the metallization inside the TSV, the back side redistribution layer (RDL) as well as the contact to the front side metal. It is shown that the front side metallization has a significant influence on the TSV contact resistance. Furthermore, the influence of different electrolytes on the Cu-Plating process (used for TSV and RDL metallization) is analyzed.

P18. Express Metrology for sub 7nm Copper and Cobalt Damascene Plating Baths

Michael Pavlov, Danni Lin, Zhi Liu, Yin Jing and Eugene Shalyt – ECI Technology, Inc.

The capability of analyzing all components in modern damascene electroplating baths using express electroanalytical methods is demonstrated. The concentration of metals in new plating baths is significantly lower than in traditional baths. This article presents the results of our most recent study of the behavior of organic additives at low metal concentrations. The newly developed methods were also applied to analysis of traditional plating baths used in damascene electroplating. The analytical results of our new methods for all bath components are presented.

THURSDAY, JUNE 30, 2022

Session 9: Advanced Interconnects

CHAIR: Todd Ryan, Zsolt Tokei

8:15 – 8:45

9.1 Recent Advances in Ni-based GeSn Metallization (Invited)

Philippe Rodriguez – CEA-Leti

In this paper, we presented an overview of the results obtained at the CEA-Leti on Ni-based GeSn metallization in the last 5 years. In particular, we discussed the solid-state reaction between a Ni thin film and GeSn layers. We then studied the behavior of the Sn during the solid-state reaction and its subsequent impact. Finally, we discussed the technological levers that can be implemented to enhance the thermal stability of the Ni / GeSn system.

8:45 – 9:15

9.2 ALD of Ru with bulk-like resistivity by balancing precursor concentration to maximum surface mobility and minimize contaminants (Invited)

Andy Kummel – UCSD

Ruthenium is viewed as a promising alternative to Cu and Co interconnect metals at M0/M1 interconnect layers due to its lower effective resistivity in highly-confined layers and vias, as well as its resistance to diffusion into porous low-k dielectrics and to electromigration. Atomic layer deposition of Ru has been reported with a variety of precursors, but the search for a Ru ALD process with a close-to-bulk (~7 μΩ·cm) resistivity is ongoing, with special interest in a process that can selectively-deposit low-resistance Ru films without passivants. In this work, Ru films with close-to-bulk resistivity deposited using Ru(CpEt)2 were investigated using four-point-probe resistivity measurements, X-ray photoelectron spectroscopy (XPS) for chemical analysis, X-ray diffraction/reflectometry (XRD/XRR) for grain size and thicknesses, and scanning electron microscopy (SEM) and atomic force microscopy (AFM) for film morphology.

9:15 – 9:40

9.3 Capacitive Impacts of Etch-Induced Dielectric Damage in Highly-Scaled Interconnect Architectures

Janet M Wilson, Nick Lanzillo – IBM

The effects of dielectric constant, damage layer thickness, line aspect ratio, and linewidth ratio on Back-End-of- Line (BEOL) line capacitance are evaluated for line pitches down to 18nm using field-solver simulations. At fine pitches such as 18nm, the damage layer thickness becomes increasingly important. We demonstrate when it may be beneficial to choose a higher-dielectric-constant material which does not create a damage layer, over a somewhat lower-dielectric-constant material. We also show the capacitive effects of metal aspect ratio, and metal width ratio, on 18nm-pitch wires.

9:40 – 10:05

9.4 Performance improvement for Cu interconnects by SAM and ELD technologies

Yuki Kikuchi – Tokyo Electron Limited

SAM (Self-Assemble-Monolayer) is a material with selectively growth on only metal or dielectric film. Moreover, SAM can have functionality such as growth inhibitory property of ALD film and Cu barrier property. The barrier/liner metal at Via bottom can be removed by SAM which has an ALD film growth inhibitory property, and by using the ELD-Cu(Electro-Less-Deposition) Pre-Via-Fill process, Cu volume at Via can be increased and Via resistance can be reduced. In this study, we have introduced the process that can reduce the process steps and reduce Via resistance by using SAM with Cu barrier properties.

10:05 – 10:30

9.5 Low Resistance Cu Vias for 24nm Pitch and Beyond

Marleen H. van der Veen, Olalla Varela Pedreira, Nicolas Jourdan, Seongho Park, Herbert Struyf, Zsolt Tokei, Carmen Leal Cervantes, Feng Chen, Xiangjin Xie, Zhiyuan Wu, Alexander Jansen, Jerome Machillot, Andrew Cockburn – IMEC

In this work we evaluate low via resistance options in 21 - 24nm pitch structures by comparing Ru, W versus Cu. A bottom barrierless Cu DD metallization is created using a selective TaN deposition. In MP24, this selective barrier Cu metallization system shows up to a 20% via resistance reduction as compared to conventional Cu DD fill with 1.5nm TaN barrier. The via resistance evaluation of the selective barrier Cu in MP21 shows that the system can be an option for further extension of Cu interconnects while keeping the resistance under control. The line and chain resistance comparison towards barrierless DD Ru shows that the SB Cu metallization is competitive in terms of performance and therefore the preferred way forward for MP24 DD structures.

10:30 – 10:50 AM Coffee Break

Session 10: DTCO

CHAIR: Zhihong Chen

10:50 – 11:20

10.1 Design-Technology Co-Optimization for BEOL Interconnect in Advanced Technologies (Invited)

Pieter Woltgens – ASML

As none-on-node simple pitch shrink diminishes as a main driver for semiconductor area shrink (and consequently density increase and cost reduction), more and more of the node-on-node area shrink needs to come from other sources, like Design-Technology Co-Optimization, in which the manufacturing process and the design get co-optimized.
As the relative importance of BEOL grows, DTCO optimizations of BEOL like standard cell design and place and route become increasingly important.
The optimizations span the full range from process (e.g. lithography) down to design and EDA. I will illustrate this DTCO approach and its impact on BEOL with two examples:
(i) a way to improve logic via printability through regularization of via placement through something we call "staggered vias", showing implementation in design as well impact on design, and experimentally demonstrated benefits for lithography, and the lithographic benefits on performance.
(ii) a proposal to make the M1 pitch gearless, liberating M1 pitch choices from the gate pitch, allowing design to more flexibly respond to the needs of PNR and BEOL patterning and lithography consequences, as well as implementation in design and impact on design.

11:20 – 11:45
10.2 EUV Minimum Pitch Single Patterning for 5nm Node Manufacturing
Jungil Park, Yun Ki Choi, Jeong Hoon Ahn, Byung Je Jung, Hoyoun Lee, Jinho Kim, Eunyoung Park, Jaehyeong Park, Hyun-Ji Song, Miji Lee, Dr. Ku, Jahum – Samsung Electronics
This paper presents a minimum pitch single patterning process for 5nm node back-end-of-line (BEOL) integration based on extreme ultraviolet (EUV) lithography with quasar illumination and optical proximity correction (OPC). OPC was applied for improving stochastic printing failures such as single-line-open (SLO) and micro-bridges. The optimized OPC effectively improved 94% of SLO and 96% of micro-bridges. The reliability requirement of the time-dependent dielectric breakdown (TDDB) was also satisfied for 5nm node BEOL integration, and this new process would be implemented for sub-5nm node device manufacturing.

11:45 – 12:10
10.3 Evaluation of BEOL scaling boosters for sub-2nm using enhanced-RO analysis
Anita Farokhnejad, Simone Esposto, Ivan Ciofi, Odysseas Zografos, Pieter Weckx, Julien Ryckaert, Pieter Schuddinck, Yang Xiang, Zsolt Tokei – IMEC
In this work, the impact of metal hybrid height (H^2) and airgap (AG) scaling boosters are evaluated based on an enhanced Ring Oscillator (RO) framework that accounts for Place and Route (PnR) aspects of the back end of line (BEOL) interconnects. When targeting best performance, extended AG with high aspect ratio (AR) lines appears to be the optimal choice as it allows reducing both capacitance (C) and resistance (R). Combining AG with H^2 provides minimum C at an increased R making it more suitable for power optimization.

12:10 – 13:30 Lunch

Session 11: DTCO and Unit Process and Integration
CHAIR: Mehul Naik, Tom Mountsier

13:30 – 13:55

11.1 Cryogenic CMOS Performance Analysis Including BEOL Characteristics at 4K for Quantum Controller Application

Koichiro Okamoto, Takahisa Tanaka, Makoto Miyamura, Hiroki Ishikuro, Ken Uchida, Toshitsugu Sakamoto, Munehiro Tada – NanoBridge Semiconductor

Cryo-CMOS circuit performance at 4K including both BEOL and FEOL characteristics has been investigated in a 65nm bulk CMOS for the first time. ON-current (Ion) of n/pMOSFET are improved +25%/+9% with excellent gate modulation (Ion/Ioff=~10^9). Cu line/via resistances decrease with temperature due to reduction of phonon scattering, and -75%/-20% lower resistances are obtained at 4K. It is revealed that there is no inter-line capacitance change and no severe Joule heating effect (JHE) of Cu BEOL at 4K. The newly developed 4K-SPICE model including BEOL characteristics enables us accurate CMOS circuit design at 4K, giving 5 ~ 40% faster operation of RC line with clear dependence on driver-size and interconnect-load.

13:55 – 14:20

11.2 Dual Damascene 28nm-Pitch Single Exposure EUV Design Rules Evaluation by Voltage Contrast Characterization

Victor M. Carballo, Dorin Cerbu, Filip Schleicher, Jeroen van de kerkhove, Philippe Leray, Nicola Kissoon, Etienne De Poortere – IMEC

In this work we have fabricated 28nm-pitch dual damascene structures using EUV single exposure for both via and metal. Ruthenium metallization has been used for the via-trench fill and final structures are characterized with Voltage Contrast metrology. By properly designing test structures with programmed shifts between via and metal and tip-to-tip variations it is possible to determine the design rules needed to obtain high yield in this process before electrical measurements.

14:20 – 14:50

11.3 Death No Moore: EUV Dry Resist for Continuous Scaling of Semiconductor Devices (Invited)

Qinghuang Lin – Lam Research

Abstract

14:50 – 15:20

11.4 Unit Process Trends and Challenges for Advanced Interconnect Scaling (Invited)

Andy Simon – IBM Research

Abstract

15:20 – 15:45

11.5 ALD Mo for Advanced MOL Local Interconnects

Maryamsadat Hosseini, Davide Tierno, Jan Willem Maes, Chiyu Zhu, Sukanya Datta, Young Byun, Moataz Mousa, Nicolas Jourdan, Eugenio Dentoni Litta, Naoto Horiguchi – IMEC

This paper introduces ALD Mo as a potential replacement for W and Co as the conductor for logic MOL interconnects. 10nm ALD Mo without a liner and barrier has a very good adhesion on SiO2, SiN and SiCO dielectrics with resistivity as low as 19-22 μΩ.cm. We demonstrate for the 1st time

a liner/barrier less ALD Mo fill capability in high aspect ratio trenches down to 10nm CD and show that ALD Mo does not drift into SiO2 and SiCO.

15:45 – 16:10

11.6 Low Resistivity Tungsten and Ruthenium through Textural Control Using Ion Beam Deposition

Rutvik Mehta, Frank Cerio, Yuejing (Crystal) Wang, Paul Turner, Jinho Kim, Ashish Kulkarni, Mohammad Saghayezhian, Robert Caldwell – VEECO

Low resistivity metal wiring and interconnects are increasingly challenged by size-dependent effects with downscaling for the next generation back end of line (BEOL) requirements. Ruthenium is considered a strong candidate although it has challenges. However, tungsten wiring is well established, widely used in DRAM, and is relatively easier to integrate. We demonstrate the novel use of ion beam deposition (IBD) to control the microstructural features, such as phase, texture, and grain size distribution of W and Ru thin films. Using IBD to drive highly selective microstructures, we have demonstrated low resistivities of <11 μΩ-cm for <20nm thick as-deposited (0001) oriented Ru and <9 μΩ-cm for <20nm thick as-deposited (110) oriented α-W. IBD deposition of W yielding epitaxial-like textured α-110 thin films was identified as showing favorable resistivity scaling. We propose the IBD of highly oriented (110) α-W as a lower cost, easily integrable solution for next generation wiring.