# 2024 IITC Workshop Program

## MONDAY, JUNE 3, 2024

## Workshop

### New dimensions to harness, upside & backside; what to consider and how to control?

**Workshop Program:**

As the conventional planar scaling of CMOS devices reaches its limits, new directions are being pursued in the vertical dimension to achieve better power, performance, and area (PPA). This shift began with the development of device architectures such as FinFETs, Nanosheets, VTFETs, and StackFETs, which extend or stack up the transistor channels vertical direction. The trend is now expanding to the interconnect/BEOL domain, where the backside of the wafer (BSPDN) and the vertical stacking of semiconductor dies (HBM) are being explored. These vertical integration techniques enable new possibilities for chip design and packaging that can improve PPA. However, they also pose new difficulties in various aspects such as wafer distortion, metrology, defect control, heat management, and reliability. These difficulties must be addressed to ensure the quality and functionality of the devices with novel structures. One of the critical areas that requires more attention is the wafer bonding and thinning process, which affects the lithography process on the wafer backside. Another significant challenge is the heat removal of the bonded wafers that lack the Si substrate. In this workshop, experts from both industry and academia will present and discuss the key technical challenges in detail associated with the 3-dimensional integration of devices, so that the audience can gain more knowledge and insights on this new and important industry trend.

9:00 – 9:15
**Welcome & Introduction**
Nick Lanzillo (Chair) – IBM Research

9:15 – 10:00
**BSPDN design considerations for advanced logic device**
Stanley S.C. Song – Google
Back-side power delivery networks (BSPDNs) is one of key enablers of technology scaling, addressing on-chip power delivery, offering a multitude of benefits for logic devices, including reduced IR drop, increased signal routing freedom, and enhanced design flexibility. This workshop presentation will delve into the details of BSPDN design, including:

- BSPDN Architectures and Implementation Options: Explore various BSPDN architectures, including Power Via, Tap Cell and Back Side Contact approaches with their implementation challenges and trade-offs.

- Impact on Logic Design, Performance, and Thermal Management: Insights into how BSPDNs influence logic design, performance metrics, and thermal considerations for High performance and mobile applications perspective.
- Design Tools, Methodologies, Reliability, and Testing: Understand the specialized design tools and methodologies tailored for BSPDN design, as well as reliability and testing strategies to ensure robust power delivery.

10:00 – 10:45

**Delivering Power and Removing Heat; Two challenges that could become the Achilles heel for AI Applications**

Madhavan Swaminathan – Penn State University

Heterogeneous Integration (HI) provides the opportunity for dense connectivity between smaller dies from advanced technology nodes to improve yield, provides for connectivity between optimized legacy technology nodes to reduce time to market, and enables the connectivity of dissimilar dies on a single platform to enhance functionality. With emerging applications in artificial intelligence (AI), the power delivery requirements are becoming astronomical while the thermal management solutions are becoming increasingly challenging. These two issues could very well become the Achilles heel for AI applications, unless appropriate solutions are sought and developed using HI.

This presentation will cover some of the emerging challenges in these areas along with solutions being pursued.

**10:45 – 11:15 Coffee Break**

11:15 – 12:00

**Advanced packaging solutions for high performance memory**

Kunal Parekh – Micron

The appetite for new applications in computing such as AI, automotive applications, and more efficient computing, are driving the need for memory and logic to rethink the architectures of both processing logic and memory, and resulting in new advanced packaging innovations that enable the future of 2.5D and 3D solutions. In this talk technology enabling interconnect and packaging and solutions will be discussed.

**12:00 – 1:00 Lunch**

1:00 – 1:45

**Wafer bonding: hybrid/fusion bonding**

Ilseok Son – TEL

Wafer bonding is one of key modules in 3DI/HI (3D Integration & Heterogeneous Integration) proving for a next generation scaling resolution path through BSPDN (Backside Power Delivery Network) & sequential CFET in logic, 3D Xtacking in NAND flash, multilayer stacking in HBM (High bandwidth memory). In this talk, wafer bonding type, process flow, and challenges in 3DI bonding will be introduced and TEL's research work on the challenges will be discussed. This discussion covers wide range of topics including incoming wafer condition's impact on bonding

void & alignment, plasma surface activation modeling & yield impact, bonding alignment impact on e-test with 0.5um pitch hybrid bonding, Cu recess/ oxidation characterization & resolution, Cu anneal expansion modeling, improved bonding energy measurement method, and wafer distortion modeling.

1:45 – 2:30

**Backside patterning from lithography perspective: alignment, metrology and overlay control**

Michale Kubis – ASML

Lithography resolution has been driving dimensional scaling of semiconductor devices, but nowadays it is more and more complemented with device level 3D architectures (such as Gate-all-around) and system level 3D integration (such as stacked SRAM on Logic). Logic backside power delivery network (BS-PDN) is a disruptive innovation that offers significant performance gain in combination with higher transistor density. Key feature of this technology is the ability to connect to the already fully processed front-end devices from the backside. This connection takes place after fusion bonding and requires, depending on the chosen process flow, a single digit tight post-bonding scanner overlay control.

In this presentation, we will discuss implications of the BS-PDN processing on scanner alignment, overlay metrology, and overlay control for the post-bonding exposures. We will show that a significant improvement is possible to meet the overlay performance requirement by applying high order corrections per exposure of the scanner and we will discuss additional opportunities to improve the performance. We will pay special attention to the wafer edge (R > 135mm) as in this region it will be most challenging to achieve the required post-bonding overlay.

**2:30 – 3:00 Coffee Break**

3:00 – 3:45

**Wafer warpage control by film deposition**

Fayaz Shaikh – LAM Research

While high aspect ratio deposition and etching are key enablers for 3D NAND scaling, the combination of increasing the number of layers while controlling wafer bow due to cumulative stress in the film stack has become a major challenge. Such stress-induced wafer distortion has a significant impact on wafer yield due to degraded lithography depth-of-focus, overlay performance, and structural distortion. To improve overall yield, wafer-, die-, and feature-level stresses need to be carefully managed at various steps throughout the entire manufacturing process flow, at times potentially resulting in the preclusion of otherwise performance-enhancing process steps due to their stress characteristics.

Designed to provide a cost-effective solution for controlling wafer bow in 3D NAND manufacturing, VECTOR DT provides a single-step solution for wafer shape management by depositing a tunable counter-stress film on the back of the wafer without contacting the front side, thereby enabling improved lithography results, reduced bow-induced failures, and integration of high performance but highly stressed films. With strong customer adoption since its debut, the VECTOR DT installed base continues to grow as customers are transitioning to more than 200 layers.

This talk will discuss the challenges of wafer shape/warpage in 3DNAND manufacturing and how backside engineering via deposition can solve and manage the wafer shape using VECTOR® DT.

**3:45 – 4:30 Roundtable Discussion**
Nick (Chair) – IBM Research, Stanley S.C. Song – Google, Madhavan Swaminathan – Penn State University, Kunal Parekh – Micron, Michale Kubis – ASML, Fayaz Shaikh – LAM Research

**4:30 – 4:45 Final Reflections**
Nick Lanzillo (Chair) – IBM Research